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1 CO and Architecture (192)

Machine instructions and Addressing modes. ALU, data-path and control unit. Instruction pipelining. Memory hierarchy: cache, main memory and secondary storage; I/O interface (Interrupt and DMA mode)

1.1 Addressing Modes (18)

1.1.1 Addressing Modes: GATE1987-1-V

https://gateoverflow.in/80194

The most relevant addressing mode to write position-independent codes is:

A. Direct mode B. Indirect mode C. Relative mode D. Indexed mode

gate1987 co-and-architecture addressing-modes

1.1.2 Addressing Modes: GATE1988-9iii

https://gateoverflow.in/94388

In the program scheme given below indicate the instructions containing any operand needing relocation for position independent behaviour. Justify your answer.

$$
\begin{array}{lll}
Y = 10 & & \\
\text{MOV} & X(R_0), R_1 & \\
\text{MOV} & X, R_0 & \\
\text{MOV} & 2(R_0), R_1 & \\
\text{MOV} & Y(R_0), R_5 & \\
& \vdots & \\
X: & \text{WORD} & 0, 0, 0
\end{array}
$$

gate1988 normal descriptive co-and-architecture addressing-modes

1.1.3 Addressing Modes: GATE1989-2-ii

https://gateoverflow.in/87078

Match the pairs in the following questions:

(A)	Base addressing	(p)	Reentranecy
(B)	Indexed addressing	(q)	Accumulator
(C)	Stack addressing	(r)	Array
(D)	Implied addressing	(s)	Position independent

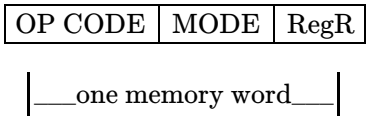
A-S, B-R, C-P, D-Q

gate1989 match-the-following co-and-architecture addressing-modes easy

1.1.4 Addressing Modes: GATE1993-10

https://gateoverflow.in/2307

The instruction format of a CPU is:



Mode and RegR together specify the operand. RegR specifies a CPU register and Mode specifies an addressing mode. In particular, Mode $= 2$ specifies that 'the register RegR contains the address of the operand, after fetching the operand, the contents of RegR are incremented by 1'.

An instruction at memory location 2000 specifies Mode $= 2$ and the RegR refers to program counter (PC).

A. What is the address of the operand?

B. Assuming that is a non-jump instruction, what are the contents of PC after the execution of this instruction?

gate1993 co-and-architecture addressing-modes normal

1.1.5 Addressing Modes: GATE1996-1.16, ISRO2016-42

https://gateoverflow.in/2720

Relative mode of addressing is most relevant to writing:

A. Co – routines
B. Position – independent code
C. Shareable code
D. Interrupt Handlers

gate1996 co-and-architecture addressing-modes easy isro2016

1.1.6 Addressing Modes: GATE1998-1.19

https://gateoverflow.in/1656

Which of the following addressing modes permits relocation without any change whatsoever in the code?

A. Indirect addressing
B. Indexed addressing
C. Base register addressing
D. PC relative addressing

gate1998 co-and-architecture addressing-modes easy

1.1.7 Addressing Modes: GATE1999-2.23

https://gateoverflow.in/1500

A certain processor supports only the immediate and the direct addressing modes. Which of the following programming language features cannot be implemented on this processor?

A,B, C requires base and index addresses

A. Pointers
B. Arrays
C. Records
D. Recursive procedures with local variable

gate1999 co-and-architecture addressing-modes normal

1.1.8 Addressing Modes: GATE2000-1.10

https://gateoverflow.in/633

The most appropriate matching for the following pairs

X: Indirect addressing	1: Loops
Y: Immediate addressing	2: Pointers
Z: Auto decrement addressing	3: Constants

is

A. $X-3, Y-2, Z-1$
B. $X-1, Y-3, Z-2$
C. $X-2, Y-3, Z-1$
D. $X-3, Y-1, Z-2$

gate2000 co-and-architecture normal addressing-modes

1.1.9 Addressing Modes: GATE2001-2.9

https://gateoverflow.in/727

Which is the most appropriate match for the items in the first column with the items in the second column:

X.	Indirect Addressing	I.	Array implementation
Y.	Indexed Addressing	II.	Writing relocatable code
Z.	Base Register Addressing	III.	Passing array as parameter

A. (X, III), (Y, I), (Z, II)
B. (X, II), (Y, III), (Z, I)
C. (X, III), (Y, II), (Z, I)
D. (X, I), (Y, III), (Z, II)

gate2001 co-and-architecture addressing-modes normal

1.1.10 Addressing Modes: GATE2002-1.24

https://gateoverflow.in/829

In the absolute addressing mode:

A. the operand is inside the instruction
B. the address of the operand in inside the instruction
C. the register containing the address of the operand is specified inside the instruction
D. the location of the operand is implicit

gate2002 co-and-architecture addressing-modes easy

1.1.11 Addressing Modes: GATE2004-20

https://gateoverflow.in/1017

Which of the following addressing modes are suitable for program relocation at run time?

I. Absolute addressing
II. Based addressing
III. Relative addressing
IV. Indirect addressing

A. I and IV
B. I and II
C. II and III
D. I, II and IV

gate2004 co-and-architecture addressing-modes easy

1.1.12 Addressing Modes: GATE2005-65

https://gateoverflow.in/1388

Consider a three word machine instruction

$ADDA[R_0], @B$

The first operand (destination) "$A[R_0]$" uses indexed addressing mode with R_0 as the index register. The second operand (source) "$@B$" uses indirect addressing mode. A and B are memory addresses residing at the second and third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is:

A. 3 B. 4 C. 5 D. 6

gate2005 co-and-architecture addressing-modes normal

1.1.13 Addressing Modes: GATE2005-66

https://gateoverflow.in/1389

Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side.

(1)	$A[I] = B[J]$	(a)	Indirect addressing
(2)	while $(^*A{+}{+});$	(b)	Indexed addressing
(3)	int temp $=^* x$	(c)	Auto increment

A. $(1,c),(2,b),(3,a)$
B. $(1,c),(2,c),(3,b)$
C. $(1,b),(2,c),(3,a)$
D. $(1,a),(2,b),(3,c)$

gate2005 co-and-architecture addressing-modes easy

1.1.14 Addressing Modes: GATE2006-IT-39, ISRO2009-42

https://gateoverflow.in/3578

Which of the following statements about relative addressing mode is FALSE?

A. It enables reduced instruction size
B. It allows indexing of array element with same instruction
C. It enables easy relocation of data
D. It enables faster address calculation than absolute addressing

gate2006-it co-and-architecture addressing-modes normal isro2009

1.1.15 Addressing Modes: GATE2006-IT-40

https://gateoverflow.in/3581

The memory locations $1000, 1001$ and 1020 have data values $18, 1$ and 16 respectively before the following program is executed.

```
MOVI    R_s, 1          ; Move immediate
LOAD    R_d, 1000(R_s)  ; Load from memory
ADDI    R_d, 1000       ; Add immediate
STOREI  0(R_d), 20      ; Store immediate
```

Which of the statements below is TRUE after the program is executed ?

A. Memory location 1000 has value 20
B. Memory location 1020 has value 20
C. Memory location 1021 has value 20
D. Memory location 1001 has value 20

gate2006-it co-and-architecture addressing-modes normal

1.1.16 Addressing Modes: GATE2008-33, ISRO2009-80

https://gateoverflow.in/444

Which of the following is/are true of the auto-increment addressing mode?

I. It is useful in creating self-relocating code
II. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation
III. The amount of increment depends on the size of the data item accessed

A. I only B. II only C. III only D. II and III only

gate2008 addressing-modes co-and-architecture normal isro2009

1.1.17 Addressing Modes: GATE2011-21

https://gateoverflow.in/2123

Consider a hypothetical processor with an instruction of type LW R1, 20(R2), which during execution reads a $32-bit$ word from memory and stores it in a $32-bit$ register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for the operand in memory?

A. Immediate addressing
B. Register addressing
C. Register Indirect Scaled Addressing
D. Base Indexed Addressing

gate2011 co-and-architecture addressing-modes easy

1.1.18 Addressing Modes: GATE2017-1-11

https://gateoverflow.in/118291

Consider the C struct defined below:

```
struct data {
    int marks [100];
    char grade;
    int cnumber;
};
struct data student;
```

The base address of student is available in register $R1$. The field student.grade can be accessed efficiently using:

A. Post-increment addressing mode, $(R1)+$
B. Pre-decrement addressing mode, $-(R1)$
C. Register direct addressing mode, $R1$
D. Index addressing mode, $X(R1)$, where X is an offset represented in $2's$ complement $16-bit$ representation

gate2017-1 co-and-architecture addressing-modes

1.2 Cache Memory (57)

1.2.1 Cache Memory: GATE1987-4b

https://gateoverflow.in/81360

What is cache memory? What is rationale of using cache memory?

gate1987 co-and-architecture cache-memory

1.2.2 Cache Memory: GATE1990-7a

https://gateoverflow.in/85403

A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of $16,384$ blocks and each block contains 256 eight bit words.

1. How many bits are required for addressing the main memory?
2. How many bits are needed to represent the TAG, SET and WORD fields?

gate1990 descriptive co-and-architecture cache-memory

1.2.3 Cache Memory: GATE1992-5-a

https://gateoverflow.in/584

The access times of the main memory and the Cache memory, in a computer system, are $500\ nsec$ and $50\ nsec$, respectively. It is estimated that 80% of the main memory request are for read the rest for write. The hit ratio for the read access only is 0.9 and a write-through policy (where both main and cache memories are updated simultaneously) is used. Determine the average time of the main memory (in ns)

gate1992 co-and-architecture cache-memory normal numerical-answers

1.2.4 Cache Memory: GATE1993-11

https://gateoverflow.in/2308

In the three-level memory hierarchy shown in the following table, p_i denotes the probability that an access request will refer to M_i.

Hierarchy Level (M_i)	Access Time (t_i)	Probability of Access (p_i)	Page Transfer Time (T_i)
M_1	10^{-6}	0.99000	0.001 sec
M_2	10^{-5}	0.00998	0.1 sec
M_3	10^{-4}	0.00002	---

If a miss occurs at level M_i, a page transfer occurs from M_{i+1} to M_i and the average time required for such a page swap is T_i. Calculate the average time t_A required for a processor to read one word from this memory system.

gate1993 co-and-architecture cache-memory normal

1.2.5 Cache Memory: GATE1995-1.6

https://gateoverflow.in/2593

The principle of locality justifies the use of:

A. Interrupts B. DMA C. Polling D. Cache Memory

gate1995 co-and-architecture cache-memory easy

1.2.6 Cache Memory: GATE1995-2.25

https://gateoverflow.in/2638

A computer system has a $4\ K$ word cache organized in block-set-associative manner with 4 blocks per set, 64 words per block. The number of bits in the SET and WORD fields of the main memory address format is:

A. $15, 40$ B. $6, 4$ C. $7, 2$ D. $4, 6$

gate1995 co-and-architecture cache-memory normal

1.2.7 Cache Memory: GATE1996-26

https://gateoverflow.in/2778

A computer system has a three-level memory hierarchy, with access time and hit ratios as shown below:

Level 1 (Cache memory)Access time $= 50 nsec/byte$

Size	Hit ratio
$8M$ bytes	0.80
$16M$ bytes	0.90
$64M$ bytes	0.95

Level 2 (Main memory)Access time $= 200 nsec/byte$

Size	Hit ratio
$4M$ bytes	0.98
$16M$ bytes	0.99
$64M$ bytes	0.995

Level 3Access time $= 5\mu$sec/byte

Size	Hit ratio
$260M$ bytes	1.0

A. What should be the minimum sizes of level 1 and 2 memories to achieve an average access time of less than $100 nsec$?

B. What is the average access time achieved using the chosen sizes of level 1 and level 2 memories?

gate1996 co-and-architecture cache-memory normal

1.2.8 Cache Memory: GATE1998-18

https://gateoverflow.in/1732

For a set-associative Cache organization, the parameters are as follows:

t_c	Cache Access Time
t_m	Main memory access time
l	Number of sets
b	Block size
$k \times b$	Set size

Calculate the hit ratio for a loop executed 100 times where the size of the loop is $n \times b$, and $n = k \times m$ is a non-zero integer and $1 < m \leq l$.

Give the value of the hit ratio for $l = 1$.

gate1998 co-and-architecture cache-memory descriptive

1.2.9 Cache Memory: GATE1999-1.22

https://gateoverflow.in/1475

The main memory of a computer has $2\ cm$ blocks while the cache has $2c$ blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block k of the main memory maps to the set:

A. $(k\ mod\ m)$ of the cache
B. $(k\ mod\ c)$ of the cache
C. $(k\ mod\ 2c)$ of the cache
D. $(k\ mod\ 2cm)$ of the cache

gate1999 co-and-architecture cache-memory normal

1.2.10 Cache Memory: GATE2001-1.7, ISRO2008-18

https://gateoverflow.in/700

More than one word are put in one cache block to:

A. exploit the temporal locality of reference in a program
B. exploit the spatial locality of reference in a program
C. reduce the miss penalty
D. none of the above

gate2001 co-and-architecture easy cache-memory isro2008

1.2.11 Cache Memory: GATE2001-9

https://gateoverflow.in/750

A CPU has $32 - bit$ memory address and a $256\ KB$ cache memory. The cache is organized as a $4 - way$ set associative cache with cache block size of 16 bytes.

A. What is the number of sets in the cache?
B. What is the size (in bits) of the tag field per cache block?
C. What is the number and size of comparators required for tag matching?
D. How many address bits are required to find the byte offset within a cache block?
E. What is the total amount of extra memory (in bytes) required for the tag bits?

extra memory= tag-memory

gate2001 co-and-architecture cache-memory normal descriptive

1.2.12 Cache Memory: GATE2002-10

https://gateoverflow.in/863

In a C program, an array is declared as $\text{float}\ A[2048]$. Each array element is 4 Bytes in size, and the starting address of the array is $0x00000000$. This program is run on a computer that has a direct mapped data cache of size 8 Kbytes, with block (line) size of 16 Bytes.

A. Which elements of the array conflict with element $A[0]$ in the data cache? Justify your answer briefly.
B. If the program accesses the elements of this array one by one in reverse order i.e., starting with the last element and ending with the first element, how many data cache misses would occur? Justify your answer briefly. Assume that the data cache is initially empty and that no other data or instruction accesses are to be considered.

gate2002 co-and-architecture cache-memory normal descriptive

1.2.13 Cache Memory: GATE2004-65

https://gateoverflow.in/1059

Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is:

$8, 12, 0, 12, 8.$

A. 2 B. 3 C. 4 D. 5

gate2004 co-and-architecture cache-memory normal

1.2.14 Cache Memory: GATE2004-IT-12, ISRO2016-77

https://gateoverflow.in/3653

Consider a system with 2 level cache. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns, 10 ns, and 500 ns respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9, respectively. What is the average access time of the system ignoring the search time within the cache?

h1.t1+ (1-h1) h2(t1+t2) +(1-h1)(1-h2)(t1+t2+tm)

A. 13.0 B. 12.8 C. 12.6 D. 12.4

Hierarchical Access is being used

gate2004-it co-and-architecture cache-memory normal isro2016

1.2.15 Cache Memory: GATE2004-IT-48

https://gateoverflow.in/3691

Consider a fully associative cache with 8 cache blocks (numbered $0 - 7$) and the following sequence of memory block requests:

$4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7$

If LRU replacement policy is used, which cache block will have memory block 7?

A. 4 B. 5 C. 6 D. 7

gate2004-it co-and-architecture cache-memory normal

1.2.16 Cache Memory: GATE2005-67

https://gateoverflow.in/1390

Consider a direct mapped cache of size 32 KB with block size 32 $bytes$. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively,

A. 10, 17 B. 10, 22 C. 15, 17 D. 5, 17

gate2005 co-and-architecture cache-memory easy

1.2.17 Cache Memory: GATE2005-IT-61

https://gateoverflow.in/3822

Consider a 2-way set associative cache memory with 4 sets and total 8 cache blocks $(0 - 7)$ and a main memory with 128 blocks $(0 - 127)$. What memory blocks will be present in the cache after the following sequence of memory block references if **LRU** policy is used for cache block replacement. Assuming that initially the cache did not have any memory block from the current job?

0 5 3 9 7 0 16 55

A. 0 3 5 7 16 55 B. 0 3 5 7 9 16 55
C. 0 5 7 9 16 55 D. 3 5 7 9 16 55

gate2005-it co-and-architecture cache-memory normal

1.2.18 Cache Memory: GATE2006-74

https://gateoverflow.in/1851

Consider two cache organizations. First one is 32 KB $2 - way$ set associative with 32 $byte$ block size, the second is of same size but direct mapped. The size of an address is 32 $bits$ in both cases . A $2 - to - 1$ multiplexer has latency of 0.6 ns while a $k - bit$ comparator has latency of $\frac{k}{10} ns$. The hit latency of the set associative organization is h_1 while that of direct mapped is h_2.

The value of h_1 is:

A. 2.4 ns B. 2.3 ns
C. 1.8 ns D. 1.7 ns

gate2006 co-and-architecture cache-memory normal

1.2.19 Cache Memory: GATE2006-75

https://gateoverflow.in/43565

Consider two cache organizations. First one is $32\ kB$ 2-way set associative with $32\ byte$ block size, the second is of same size but direct mapped. The size of an address is $32\ bits$ in both cases . A 2-to-1 multiplexer has latency of $0.6ns$ while a $k-$bit comparator has latency of $\frac{k}{10}ns$. The hit latency of the set associative organization is h_1 while that of direct mapped is h_2.
The value of h_2 is:

A. $2.4\ ns$ B. $2.3\ ns$ C. $1.8\ ns$ D. $1.7\ ns$

gate2006 co-and-architecture cache-memory normal

1.2.20 Cache Memory: GATE2006-80

https://gateoverflow.in/1854

A CPU has a $32KB$ direct mapped cache with 128 byte-block size. Suppose A is two dimensional array of size 512×512 with elements that occupy 8-bytes each. Consider the following two C code segments, $P1$ and $P2$.

P1:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[i] [j];
    }
}
```

P2:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[j] [i];
    }
}
```

$P1$ and $P2$ are executed independently with the same initial state, namely, the array A is not in the cache and
i,
j,
x are in registers. Let the number of cache misses experienced by $P1$ be M_1 and that for $P2$ be M_2.
The value of M_1 is:

A. 0 B. 2048 C. 16384 D. 262144

gate2006 co-and-architecture cache-memory normal

1.2.21 Cache Memory: GATE2006-81

https://gateoverflow.in/43517

A **CPU** has a $32\ KB$ direct mapped cache with 128 byte-block size. Suppose A is two dimensional array of size 512×512 with elements that occupy $8 - bytes$ each. Consider the following two C code segments, $P1$ and $P2$.
$P1$:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[i] [j];
    }
}
```

P2:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[j] [i];
    }
}
```

$P1$ and $P2$ are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by $P1$ be $M1$ and that for $P2$ be $M2$.

The value of the ratio $\frac{M_1}{M_2}$:

A. 0 B. $\frac{1}{16}$ C. $\frac{1}{8}$ D. 16

co-and-architecture cache-memory normal gate2006

1.2.22 Cache Memory: GATE2006-IT-42

https://gateoverflow.in/3585

A cache line is 64 bytes. The main memory has latency $32\ ns$ and bandwidth $1\ GBytes/s$. The time required to fetch the entire cache line from the main memory is:

A. $32\ ns$ B. $64\ ns$ C. $96\ ns$ D. $128\ ns$

gate2006-it co-and-architecture cache-memory normal

1.2.23 Cache Memory: GATE2006-IT-43

https://gateoverflow.in/3586

A computer system has a level-1 instruction cache (1-cache), a level-1 data cache (D-cache) and a level-2 cache ($L2$-cache) with the following specifications:

	Capacity	**Mapping Method**	**Block Size**
I-Cache	$4K$ words	Direct mapping	4 words
D-Cache	$4K$ words	2 -way set associative mapping	4 words
$L2$-Cache	$64K$ words	4-way set associative mapping	16 words

The length of the physical address of a word in the main memory is 30 bits. The capacity of the tag memory in the I-cache, D-cache and $L2$-cache is, respectively,

A. 1 K x 18-bit, 1 K x 19-bit, 4 K x 16-bit
B. 1 K x 16-bit, 1 K x 19-bit, 4 K x 18-bit
C. 1 K x 16-bit, 512 x 18-bit, 1 K x 16-bit
D. 1 K x 18-bit, 512 x 18-bit, 1 K x 18-bit

gate2006-it co-and-architecture cache-memory normal

1.2.24 Cache Memory: GATE2007-10

https://gateoverflow.in/1208

Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The **CPU** generates a $20-bit$ address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively:

A. $9, 6, 5$ B. $7, 7, 6$ C. $7, 5, 8$ D. $9, 5, 6$

gate2007 co-and-architecture cache-memory normal

1.2.25 Cache Memory: GATE2007-80

https://gateoverflow.in/1273

Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of $64\ bytes$ each is used in the system. A 50 x 50 two-dimensional array of bytes is stored in the main memory starting from memory location $1100H$. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

How many data misses will occur in total?

A. 48 B. 50 C. 56 D. 59

gate2007 co-and-architecture cache-memory normal

1.2.26 Cache Memory: GATE2007-81

https://gateoverflow.in/43511

Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50 x 50 two-dimensional array of bytes is stored in the main memory starting from memory location $1100H$. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

Which of the following lines of the data cache will be replaced by new blocks in accessing the array for the second time?

A. line 4 to line 11
B. line 4 to line 12
C. line 0 to line 7
D. line 0 to line 8

gate2007 co-and-architecture cache-memory normal

1.2.27 Cache Memory: GATE2007-IT-37

https://gateoverflow.in/3470

Consider a Direct Mapped Cache with 8 cache blocks (numbered $0-7$). If the memory block requests are in the following order

$3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24.$

Which of the following memory blocks will not be in the cache at the end of the sequence ?

A. 3 B. 18 C. 20 D. 30

gate2007-it co-and-architecture cache-memory normal

1.2.28 Cache Memory: GATE2008-35

https://gateoverflow.in/446

For inclusion to hold between two cache levels L_1 and L_2 in a multi-level cache hierarchy, which of the following are necessary?

I. L_1 must be write-through cache
II. L_2 must be a write-through cache
III. The associativity of L_2 must be greater than that of L_1
IV. The L_2 cache must be at least as large as the L_1 cache

A. IV only B. I and IV only C. I, II and IV only D. I, II, III and IV

gate2008 co-and-architecture cache-memory normal

1.2.29 Cache Memory: GATE2008-71

https://gateoverflow.in/494

Consider a machine with a 2-way set associative data cache of size 64 $Kbytes$ and block size 16 $bytes$. The cache is managed using 32 bit virtual addresses and the page size is 4 $Kbytes$. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page $0xFF000$ and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

The total size of the tags in the cache directory is:

A. 32 $Kbits$ B. 34 $Kbits$ C. 64 $Kbits$ D. 68 $Kbits$

gate2008 co-and-architecture cache-memory normal

1.2.30 Cache Memory: GATE2008-72

https://gateoverflow.in/43490

Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page $0xFF000$ and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

Which of the following array elements have the same cache index as $ARR[0][0]$?

A. $ARR[0][4]$ B. $ARR[4][0]$ C. $ARR[0][5]$ D. $ARR[5][0]$

gate2008 co-and-architecture cache-memory normal

1.2.31 Cache Memory: GATE2008-73

https://gateoverflow.in/43491

Consider a machine with a 2-way set associative data cache of size 64 $Kbytes$ and block size 16 $bytes$. The cache is managed using 32 bit virtual addresses and the page size is 4 $Kbytes$. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page $0xFF000$ and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

The cache hit ratio for this initialization loop is:

A. 0% B. 25% C. 50% D. 75%

gate2008 co-and-architecture cache-memory normal

1.2.32 Cache Memory: GATE2008-IT-80

https://gateoverflow.in/3403

Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB.

The number of bits in the TAG, SET and WORD fields, respectively are:

A. $7, 6, 7$ B. $8, 5, 7$ C. $8, 6, 6$ D. $9, 4, 7$

gate2008-it co-and-architecture cache-memory normal

1.2.33 Cache Memory: GATE2008-IT-81

https://gateoverflow.in/3405

Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 $byte$, a block size of 128 words and a cache size of 8 KB.

While accessing the memory location $0C795H$ by the **CPU**, the contents of the TAG field of the corresponding cache line is:

A. 000011000 B. 110001111 C. 00011000 D. 110010101

gate2008-it co-and-architecture cache-memory normal

1.2.34 Cache Memory: GATE2009-29

https://gateoverflow.in/1315

Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks are in the following order:

$0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155.$

Which one of the following memory block will NOT be in cache if LRU replacement policy is used?

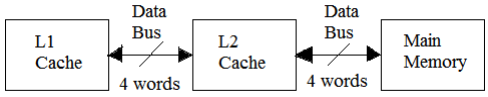
A. 3 B. 8 C. 129 D. 216

gate2009 co-and-architecture cache-memory normal

1.2.35 Cache Memory: GATE2010-48

https://gateoverflow.in/2352

A computer system has an $L1$ cache, an $L2$ cache, and a main memory unit connected as shown below. The block size in $L1$ cache is 4 words. The block size in $L2$ cache is 16 words. The memory access times are 2 $nanoseconds$, 20 $nanoseconds$ and 200 $nanoseconds$ for $L1$ cache, $L2$ cache and the main memory unit respectively.



When there is a miss in $L1$ cache and a hit in $L2$ cache, a block is transferred from $L2$ cache to $L1$ cache. What is the time

taken for this transfer?

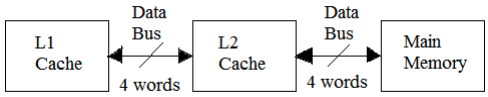
A. $2\,nanoseconds$
B. $20\,nanoseconds$
C. $22\,nanoseconds$
D. $88\,nanoseconds$

gate2010 co-and-architecture cache-memory normal barc2017

1.2.36 Cache Memory: GATE2010-49

https://gateoverflow.in/43329

A computer system has an $L1$ cache, an $L2$ cache, and a main memory unit connected as shown below. The block size in $L1$ cache is 4 words. The block size in $L2$ cache is 16 words. The memory access times are $2\,$nanoseconds, $20\,$nanoseconds and $200\,$nanoseconds for $L1$ cache, $L2$ cache and the main memory unit respectively.



When there is a miss in both $L1$ cache and $L2$ cache, first a block is transferred from main memory to $L2$ cache, and then a block is transferred from $L2$ cache to $L1$ cache. What is the total time taken for these transfers?

A. $222\,$nanoseconds
B. $888\,$nanoseconds
C. $902\,$nanoseconds
D. $968\,$nanoseconds

gate2010 co-and-architecture cache-memory normal

1.2.37 Cache Memory: GATE2011-43

https://gateoverflow.in/2145

An $8KB$ direct-mapped write-back cache is organized as multiple blocks, each size of 32-$bytes$. The processor generates 32-bit addresses. The cache controller contains the tag information for each cache block comprising of the following.

- 1 valid bit
- 1 modified bit
- As many bits as the minimum needed to identify the memory block mapped in the cache.

What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

A. $4864\ bits$
B. $6144\ bits$
C. $6656\ bits$
D. $5376\ bits$

gate2011 co-and-architecture cache-memory normal

1.2.38 Cache Memory: GATE2012-54

https://gateoverflow.in/2192

A computer has a 256-KByte, 4-way set associative, write back data cache with block size of 32-Bytes. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The number of bits in the tag field of an address is

A. 11
B. 14
C. 16
D. 27

gate2012 co-and-architecture cache-memory normal

1.2.39 Cache Memory: GATE2012-55

https://gateoverflow.in/43311

A computer has a 256-KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The size of the cache tag directory is:

A. 160 Kbits
B. 136 Kbits
C. 40 Kbits
D. 32 Kbits

normal gate2012 co-and-architecture cache-memory

1.2.40 Cache Memory: GATE2013-20

https://gateoverflow.in/1442

In a k-way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set $(s+1)$. The main memory blocks are numbered 0 onwards. The main memory block numbered j must be mapped to any one of the cache lines from

A. $(j \bmod v) * k$ to $(j \bmod v) * k + (k-1)$
B. $(j \bmod v)$ to $(j \bmod v) + (k-1)$
C. $(j \bmod k)$ to $(j \bmod k) + (v-1)$
D. $(j \bmod k) * v$ to $(j \bmod k) * v + (v-1)$

gate2013 co-and-architecture cache-memory normal

1.2.41 Cache Memory: GATE2014-1-44

https://gateoverflow.in/1922

An access sequence of cache block addresses is of length N and contains n unique block addresses. The number of unique block addresses between two consecutive accesses to the same block address is bounded above by k. What is the miss ratio if the access sequence is passed through a cache of associativity $A \geq k$ exercising least-recently-used replacement policy?

A. $\left(\frac{n}{N}\right)$ B. $\left(\frac{1}{N}\right)$ C. $\left(\frac{1}{A}\right)$ D. $\left(\frac{k}{n}\right)$

gate2014-1 co-and-architecture cache-memory normal

1.2.42 Cache Memory: GATE2014-2-43

https://gateoverflow.in/2009

In designing a computer's cache system, the cache block (or cache line) size is an important parameter. Which one of the following statements is correct in this context?

A. A smaller block size implies better spatial locality
B. A smaller block size implies a smaller cache tag and hence lower cache tag overhead
C. A smaller block size implies a larger cache tag and hence lower cache hit time
D. A smaller block size incurs a lower cache miss penalty

gate2014-2 co-and-architecture cache-memory normal

1.2.43 Cache Memory: GATE2014-2-44

https://gateoverflow.in/2010

If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?

A. Width of tag comparator
B. Width of set index decoder
C. Width of way selection multiplexer
D. Width of processor to main memory data bus

gate2014-2 co-and-architecture cache-memory normal

1.2.44 Cache Memory: GATE2014-2-9

https://gateoverflow.in/1963

A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is ____

gate2014-2 co-and-architecture cache-memory numerical-answers normal

1.2.45 Cache Memory: GATE2014-3-44

https://gateoverflow.in/2078

The memory access time is 1 $nanosecond$ for a read operation with a hit in cache, 5 $nanoseconds$ for a read operation with a miss in cache, 2 $nanoseconds$ for a write operation with a hit in cache and 10 $nanoseconds$ for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is _____.

gate2014-3 co-and-architecture cache-memory numerical-answers normal

1.2.46 Cache Memory: GATE2015-2-24

https://gateoverflow.in/8119

Assume that for a certain processor, a read request takes 50 $nanoseconds$ on a cache miss and 5 $nanoseconds$ on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a cache hit. The average read access time in nanoseconds is _____.

gate2015-2 co-and-architecture cache-memory easy numerical-answers

1.2.47 Cache Memory: GATE2015-3-14

https://gateoverflow.in/8410

Consider a machine with a byte addressable main memory of 2^{20} bytes, block size of 16 bytes and a direct mapped cache having 2^{12} cache lines. Let the addresses of two consecutive bytes in main memory be $(E201F)_{16}$ and $(E2020)_{16}$. What are the tag and cache line addresses (in hex) for main memory address $(E201F)_{16}$?

A. $E, 201$ B. $F, 201$ C. $E, E20$ D. $2, 01F$

gate2015-3 co-and-architecture cache-memory normal

1.2.48 Cache Memory: GATE2016-2-32

https://gateoverflow.in/39622

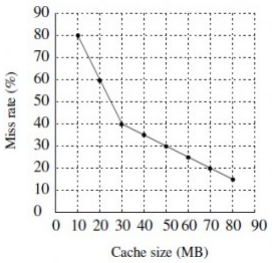
The width of the physical address on a machine is 40 bits. The width of the tag field in a 512 KB 8-way set associative cache is _____ bits.

gate2016-2 co-and-architecture cache-memory normal numerical-answers

1.2.49 Cache Memory: GATE2016-2-50

https://gateoverflow.in/39592

A file system uses an in-memory cache to cache disk blocks. The miss rate of the cache is shown in the figure. The latency to read a block from the cache is 1 ms and to read a block from the disk is 10 ms. Assume that the cost of checking whether a block exists in the cache is negligible. Available cache sizes are in multiples of 10 MB.



The smallest cache size required to ensure an average read latency of less than 6 ms is _____ MB.

gate2016-2 co-and-architecture cache-memory normal numerical-answers

1.2.50 Cache Memory: GATE2017-1-25

https://gateoverflow.in/118305

Consider a two-level cache hierarchy with $L1$ and $L2$ caches. An application incurs 1.4 memory accesses per instruction on average. For this application, the miss rate of $L1$ cache is 0.1; the $L2$ cache experiences, on average, 7 misses per 1000 instructions. The miss rate of $L2$ expressed correct to two decimal places is _____.

gate2017-1 co-and-architecture cache-memory numerical-answers

1.2.51 Cache Memory: GATE2017-1-54

https://gateoverflow.in/118748

A cache memory unit with capacity of N words and block size of B words is to be designed. If it is designed as a direct mapped cache, the length of the TAG field is 10 bits. If the cache unit is now designed as a 16-way set-associative cache, the length of the TAG field is _____ bits.

gate2017-1 co-and-architecture cache-memory normal numerical-answers

1.2.52 Cache Memory: GATE2017-2-29

https://gateoverflow.in/118371

In a two-level cache system, the access times of L_1 and L_2 caches are 1 and 8 clock cycles, respectively. The miss penalty from the L_2 cache to main memory is 18 clock cycles. The miss rate of L_1 cache is twice that of L_2. The average memory access time (AMAT) of this cache system is 2 cycles. The miss rates of L_1 and L_2 respectively are

A. 0.111 and 0.056 B. 0.056 and 0.111 C. 0.0892 and 0.1784 D. 0.1784 and 0.0892

gate2017-2 cache-memory co-and-architecture normal

AMAT = Hit_TimeL1 + MissRateL1*(HitTimeL2 + MissRateL2*Miss_PenaltyL2)

1.2.53 Cache Memory: GATE2017-2-45

https://gateoverflow.in/118597

The read access times and the hit ratios for different caches in a memory hierarchy are as given below:

Cache	Read access time (in nanoseconds)	Hit ratio
I-cache	2	0.8
D-cache	2	0.9
$L2$-cache	8	0.9

The read access time of main memory in 90 nanoseconds. Assume that the caches use the referred-word-first read policy and the write-back policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In execution of a program, 60% of memory reads are for instruction fetch and 40% are for memory operand fetch. The average read access time in nanoseconds (up to 2 decimal places) is _____

gate2017-2 co-and-architecture cache-memory numerical-answers

1.2.54 Cache Memory: GATE2017-2-53 https://gateoverflow.in/118613

Consider a machine with a byte addressable main memory of 2^{32} bytes divided into blocks of size 32 bytes. Assume that a direct mapped cache having 512 cache lines is used with this machine. The size of the tag field in bits is _____

gate2017-2 co-and-architecture cache-memory numerical-answers

1.2.55 Cache Memory: GATE2018-34 https://gateoverflow.in/204108

The size of the physical address space of a processor is 2^P bytes. The word length is 2^W bytes. The capacity of cache memory is 2^N bytes. The size of each cache block is 2^M words. For a K-way set-associative cache memory, the length (in number of bits) of the tag field is

A. $P - N - \log_2 K$
B. $P - N + \log_2 K$
C. $P - N - M - W - \log_2 K$
D. $P - N - M - W + \log_2 K$

gate2018 co-and-architecture cache-memory normal

1.2.56 Cache Memory: GATE2019-1 https://gateoverflow.in/302847

A certain processor uses a fully associative cache of size 16 kB, The cache block size is 16 bytes. Assume that the main memory is byte addressable and uses a 32-bit address. How many bits are required for the *Tag* and the *Index* fields respectively in the addresses generated by the processor?

A. 24 bits and 0 bits
B. 28 bits and 4 bits
C. 24 bits and 4 bits
D. 28 bits and 0 bits

gate2019 co-and-architecture cache-memory normal

1.2.57 Cache Memory: GATE2019-45 https://gateoverflow.in/302803

A certain processor deploys a single-level cache. The cache block size is 8 words and the word size is 4 bytes. The memory system uses a 60-MHz clock. To service a cache miss, the memory controller first takes 1 cycle to accept the starting address of the block, it then takes 3 cycles to fetch all the eight words of the block, and finally transmits the words of the requested block at the rate of 1 word per cycle. The maximum bandwidth for the memory system when the program running on the processor issues a series of road operations is _____$\times 10^6$ bytes/sec

gate2019 numerical-answers co-and-architecture cache-memory

1.3 Cisc Risc Architecture (2)

1.3.1 Cisc Risc Architecture: GATE1999-2.22 https://gateoverflow.in/1499

The main difference(s) between a CISC and a RISC processor is/are that a RISC processor typically

A. has fewer instructions
B. has fewer addressing modes
C. has more registers
D. is easier to implement using hard-wired logic

gate1999 co-and-architecture normal cisc-risc-architecture

1.3.2 Cisc Risc Architecture: GATE2018-5 https://gateoverflow.in/204079

Consider the following processor design characteristics:

I. Register-to-register arithmetic operations only
II. Fixed-length instruction format
III. Hardwired control unit

Which of the characteristics above are used in the design of a RISC processor?

A. I and II only B. II and III only C. I and III only D. I, II and III

gate2018 co-and-architecture cisc-risc-architecture easy

1.4 Clock Frequency (2)

1.4.1 Clock Frequency: GATE1992-01-iii

https://gateoverflow.in/547

Many microprocessors have a specified lower limit on clock frequency (apart from the maximum clock frequency limit) because _____

gate1992 normal co-and-architecture clock-frequency

1.4.2 Clock Frequency: GATE2007-IT-36

https://gateoverflow.in/3469

The floating point unit of a processor using a design D takes $2t$ cycles compared to t cycles taken by the fixed point unit. There are two more design suggestions D_1 and D_2. D_1 uses 30% more cycles for fixed point unit but 30% less cycles for floating point unit as compared to design D. D_2 uses 40% less cycles for fixed point unit but 10% more cycles for floating point unit as compared to design D. For a given program which has 80% fixed point operations and 20% floating point operations, which of the following ordering reflects the relative performances of three designs?
($D_i > D_j$ denotes that D_i is faster than D_j)

A. $D_1 > D > D_2$
B. $D_2 > D > D_1$
C. $D > D_2 > D_1$
D. $D > D_1 > D_2$

gate2007-it co-and-architecture normal clock-frequency

1.5 Conflict Misses (1)

1.5.1 Conflict Misses: GATE2017-1-51

https://gateoverflow.in/118745

Consider a $2-$way set associative cache with 256 blocks and uses LRU replacement. Initially the cache is empty. Conflict misses are those misses which occur due to the contention of multiple blocks for the same cache set. Compulsory misses occur due to first time access to the block. The following sequence of access to memory blocks :

$$\{0, 128, 256, 128, 0, 128, 256, 128, 1, 129, 257, 129, 1, 129, 257, 129\}$$

is repeated 10 times. The number of *conflict misses* experienced by the cache is _____ .

gate2017-1 co-and-architecture cache-memory conflict-misses normal numerical-answers

1.6 Control Unit (1)

1.6.1 Control Unit: Gate1987-1-vi

https://gateoverflow.in/166

Microprogrammed control unit:

A. is faster than a hardwired control unit
B. facilitates easy implementation of new instructions
C. is useful when very small programs are to be run
D. usually refers to control unit of a microprocessor

gate1987 microprogramming control-unit easy co-and-architecture

1.7 Data Dependences (2)

1.7.1 Data Dependences: GATE2007-IT-39

https://gateoverflow.in/3472

Data forwarding techniques can be used to speed up the operation in presence of data dependencies. Consider the following replacements of LHS with RHS.

i. $R1 \rightarrow Loc, Loc \rightarrow R2 \equiv R1 \rightarrow R2, R1 \rightarrow Loc$
ii. $R1 \rightarrow Loc, Loc \rightarrow R2 \equiv R1 \rightarrow R2$
iii. $R1 \rightarrow Loc, R2 \rightarrow Loc \equiv R1 \rightarrow Loc$

iv. $R1 \rightarrow Loc, R2 \rightarrow Loc \quad \equiv R2 \rightarrow Loc$

In which of the following options, will the result of executing the RHS be the same as executing the LHS irrespective of the instructions that follow ?

A. i and iii
B. i and iv
C. ii and iii
D. ii and iv

gate2007-it data-dependences co-and-architecture

1.7.2 Data Dependences: GATE2015-3-47

https://gateoverflow.in/8556

Consider the following code sequence having five instructions from I_1 to I_5. Each of these instructions has the following format.

OP Ri, Rj, Rk

Where operation OP is performed on contents of registers Rj and Rk and the result is stored in register Ri.

I_1: ADD R1, R2, R3

I_2: MUL R7, R1, R3

I_3: SUB R4, R1, R5

I_4: ADD R3, R2, R4

I_5: MUL R7, R8, R9

Consider the following three statements.

S1: There is an anti-dependence between instructions I_2 and I_5

S2: There is an anti-dependence between instructions I_2 and I_4

S3: Within an instruction pipeline an anti-dependence always creates one or more stalls

Which one of the above statements is/are correct?

A. Only S1 is true
B. Only S2 is true
C. Only S1 and S3 are true
D. Only S2 and S3 are true

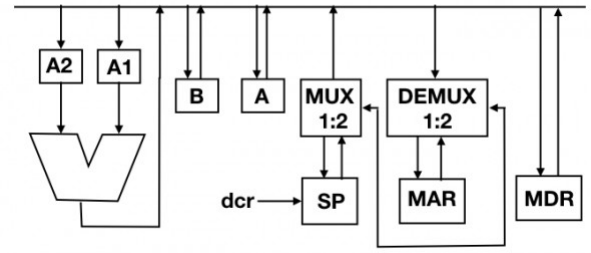
gate2015-3 co-and-architecture pipelining data-dependences normal

1.8 Data Path (4)

1.8.1 Data Path: GATE2001-2.13

https://gateoverflow.in/731

Consider the following data path of a simple non-pipelined CPU. The registers A, B, A_1, A_2, MDR, the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size $8 \times (2:1)$ and the DEMUX is of size $8 \times (1:2)$. Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and MDR (Memory Date Register). SP can be decremented locally.



The CPU instruction "push r" where, $r = A$ or B has the specification

- $M[SP] \leftarrow r$
- $SP \leftarrow SP - 1$

How many CPU clock cycles are required to execute the "push r" instruction?

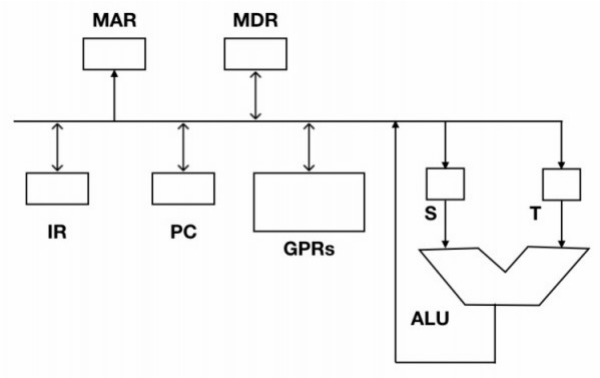
A. 2 B. 3 C. 4 D. 5

gate2001 co-and-architecture data-path machine-instructions normal

1.8.2 Data Path: GATE2005-79

https://gateoverflow.in/1402

Consider the following data path of a CPU.



The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR.

The instruction “add R0, R1” has the register transfer interpretation R0 <= R0 + R1. The minimum number of clock cycles needed for execution cycle of this instruction is:

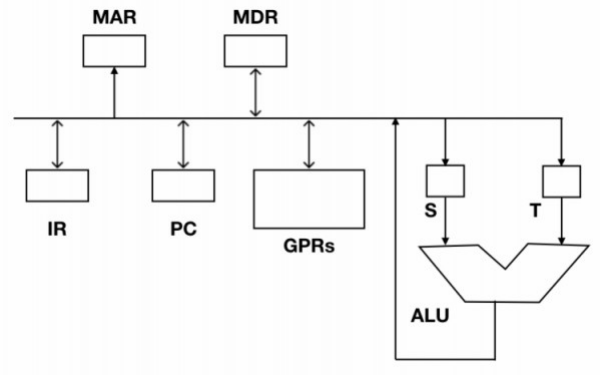
A. 2 B. 3 C. 4 D. 5

gate2005 co-and-architecture machine-instructions data-path normal

1.8.3 Data Path: GATE2005-80

https://gateoverflow.in/43568

The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR.



The instruction "call Rn, sub” is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is

$Rn \leftarrow PC + 1;$

$PC \leftarrow M[PC];$

The minimum number of **CPU** clock cycles needed during the execution cycle of this instruction is:

A. 2 B. 3 C. 4 D. 5

co-and-architecture normal gate2005 data-path machine-instructions

1.8.4 Data Path: GATE2016-2-30

https://gateoverflow.in/39627

Suppose the functions F and G can be computed in 5 and 3 nanoseconds by functional units U_F and U_G, respectively. Given two instances of U_F and two instances of U_G, it is required to implement the computation $F(G(X_i))$ for $1 \leq i \leq 10$. Ignoring all other delays, the minimum time required to complete this computation is _____ nanoseconds.

gate2016-2 co-and-architecture data-path normal numerical-answers

1.9 Dma (5)

1.9.1 Dma: GATE2004-68

https://gateoverflow.in/1062

A hard disk with a transfer rate of 10 Mbytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?

A. 5.0% B. 1.0% C. 0.5% D. 0.1%

gate2004 dma normal co-and-architecture

1.9.2 Dma: GATE2004-IT-51

https://gateoverflow.in/3694

The storage area of a disk has the innermost diameter of 10 cm and outermost diameter of 20 cm. The maximum storage density of the disk is 1400 bits/cm. The disk rotates at a speed of 4200 RPM. The main memory of a computer has 64-bit word length and 1µs cycle time. If cycle stealing is used for data transfer from the disk, the percentage of memory cycles stolen for transferring one word is

A. 0.5% B. 1% C. 5% D. 10%

gate2004-it co-and-architecture dma normal

1.9.3 Dma: GATE2005-70

https://gateoverflow.in/1393

Consider a disk drive with the following specifications:

16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one 4 byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is:

A. 10 B. 25 C. 40 D. 50

gate2005 co-and-architecture disks normal dma

1.9.4 Dma: GATE2011-28

https://gateoverflow.in/2130

On a non-pipelined sequential processor, a program segment, which is the part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

```
        Initialize the address register
        Initialize the count to 500
LOOP:   Load a byte from device
        Store in memory at address given by address register
        Increment the address register
        Decrement the count
        If count !=0 go to LOOP
```

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.

What is the approximate speed up when the DMA controller based design is used in a place of the interrupt driven program based input-output?

A. 3.4 B. 4.4 C. 5.1 D. 6.7

gate2011 co-and-architecture dma normal

1.9.5 Dma: GATE2016-1-31

https://gateoverflow.in/39698

The size of the data count register of a DMA controller is 16bits.
The processor needs to transfer a file of 29, 154 kilobytes from disk to main memory.
The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____-.

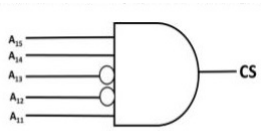
gate2016-1 co-and-architecture dma normal numerical-answers

1.10 Dram (1)

1.10.1 Dram: GATE2019-2

https://gateoverflow.in/302846

The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the memory system has 16 address lines denoted by A_{15} to A_0. What is the range of address (in hexadecimal) of the memory system that can get enabled by the chip select (CS) signal?



A. C800 to CFFF
B. CA00 to CAFF
C. C800 to C8FF
D. DA00 to DFFF

gate2019 co-and-architecture dram

1.11 Expanding Opcode (1)

1.11.1 Expanding Opcode: GATE1988-2-ii

https://gateoverflow.in/91676

Using an expanding opcode encoding for instructions, is it possible to encode all of the following in an instruction format shown in the below figure. Justify your answer.

14	double address instructions
127	single address instructions
60	no address (zero address) instructions

← 4 bits →	← 6 bits →	← 6 bits →
Opcode	Operand 1 Address	Operand 2 Address

gate1988 normal co-and-architecture expanding-opcode descriptive

1.12 Instruction Execution (6)

1.12.1 Instruction Execution: GATE1990-4-iii

https://gateoverflow.in/85391

State whether the following statements are TRUE or FALSE with reason:

The flags are affected when conditional CALL or JUMP instructions are executed.

gate1990 true-false co-and-architecture instruction-execution

1.12.2 Instruction Execution: GATE1992-01-iv

https://gateoverflow.in/548

Many of the advanced microprocessors prefetch instructions and store it in an instruction buffer to speed up processing. This speed up is achieved because _____

gate1992 co-and-architecture easy instruction-execution

1.12.3 Instruction Execution: GATE1995-1.2

https://gateoverflow.in/2589

Which of the following statements is true?

A. ROM is a Read/Write memory
B. PC points to the last instruction that was executed
C. Stack works on the principle of LIFO
D. All instructions affect the flags

gate1995 co-and-architecture normal instruction-execution

1.12.4 Instruction Execution: GATE2002-1.13

https://gateoverflow.in/817

Which of the following is not a form of memory

A. instruction cache
B. instruction register
C. instruction opcode
D. translation look-a-side buffer

gate2002 co-and-architecture easy instruction-execution

1.12.5 Instruction Execution: GATE2006-43

https://gateoverflow.in/1819

Consider a new instruction named branch-on-bit-set (mnemonic bbs). The instruction "bbs reg, pos, label" jumps to label if bit in position pos of register operand reg is one. A register is $32 - bits$ wide and the bits are numbered 0 to 31, bit in position 0 being the least significant. Consider the following emulation of this instruction on a processor that does not have bbs implemented.

$temp \leftarrow reg \& mask$

Branch to label if temp is non-zero. The variable temp is a temporary register. For correct emulation, the variable mask must be generated by

A. $mask \leftarrow 0x1 << pos$
B. $mask \leftarrow 0xffffffff << pos$
C. $mask \leftarrow pos$
D. $mask \leftarrow 0xf$

gate2006 co-and-architecture normal instruction-execution

1.12.6 Instruction Execution: GATE2017-1-49

https://gateoverflow.in/118332

Consider a RISC machine where each instruction is exactly 4 bytes long. Conditional and unconditional branch instructions use PC-relative addressing mode with Offset specified in bytes to the target location of the branch instruction. Further the Offset is always with respect to the address of the next instruction in the program sequence. Consider the following instruction sequence

Instr. No.	Instruction
i:	add R2, R3, R4
i+1:	sub R5, R6, R7
i+2:	cmp R1, R9, R10
i+3:	beq R1, Offset

If the target of the branch instruction is i, then the decimal value of the Offset is _____.

16

gate2017-1 co-and-architecture normal numerical-answers instruction-execution

1.13 Instruction Format (5)

1.13.1 Instruction Format: GATE1992-01-vi

https://gateoverflow.in/551

In an $11 - bit$ computer instruction format, the size of address field is $4 - bits$. The computer uses expanding OP code technique and has 5 two-address instructions and 32 one-address instructions. The number of zero-address instructions it can support is _____

gate1992 co-and-architecture machine-instructions instruction-format normal numerical-answers

1.13.2 Instruction Format: GATE1994-3.2

https://gateoverflow.in/2479

State True or False with one line explanation

Expanding opcode instruction formats are commonly employed in RISC. (Reduced Instruction Set Computers) machines.

gate1994 co-and-architecture machine-instructions instruction-format normal

1.13.3 Instruction Format: GATE2014-1-9

https://gateoverflow.in/1767

A machine has a $32 - bit$ architecture, with $1 - word$ long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is _____

gate2014-1 co-and-architecture machine-instructions instruction-format numerical-answers normal

1.13.4 Instruction Format: GATE2016-2-31

https://gateoverflow.in/39601

Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is _____.

gate2016-2 instruction-format machine-instructions co-and-architecture normal numerical-answers

1.13.5 Instruction Format: GATE2018-51

https://gateoverflow.in/204126

A processor has 16 integer registers $(R0, R1, \ldots, R15)$ and 64 floating point registers $(F0, F1, \ldots, F63)$. It uses a $2 - byte$ instruction format. There are four categories of instructions: $Type - 1, Type - 2, Type - 3,$ and $Type - 4$. $Type - 1$ category consists of four instructions, each with 3 integer register operands $(3Rs)$. $Type - 2$ category consists of eight instructions, each with 2 floating point register operands $(2Fs)$. $Type - 3$ category consists of fourteen instructions, each with one integer register operand and one floating point register operand $(1R + 1F)$. $Type - 4$ category consists of N instructions, each with a floating point register operand $(1F)$.

The maximum value of N is _____

gate2018 co-and-architecture machine-instructions instruction-format numerical-answers

1.14 Interrupts (6)

1.14.1 Interrupts: GATE1987-1-viii

https://gateoverflow.in/80274

On receiving an interrupt from a I/O device the CPU:

A. Halts for a predetermined time.
B. Hands over control of address bus and data bus to the interrupting device.
C. Branches off to the interrupt service routine immediately.
D. Branches off to the interrupt service routine after completion of the current instruction.

gate1987 co-and-architecture interrupts

1.14.2 Interrupts: GATE1995-1.3

https://gateoverflow.in/2590

In a vectored interrupt:

A. The branch address is assigned to a fixed location in memory
B. The interrupting source supplies the branch information to the processor through an interrupt vector
C. The branch address is obtained from a register in the processor
D. None of the above

gate1995 co-and-architecture interrupts normal

1.14.3 Interrupts: GATE1998-1.20

https://gateoverflow.in/1657

Which of the following is true?

A. Unless enabled, a CPU will not be able to process interrupts.
B. Loop instructions cannot be interrupted till they complete.
C. A processor checks for interrupts before executing a new instruction.
D. Only level triggered interrupts are possible on microprocessors.

gate1998 co-and-architecture interrupts normal

1.14.4 Interrupts: GATE2002-1.9

https://gateoverflow.in/813

A device employing INTR line for device interrupt puts the CALL instruction on the data bus while:

A. $\overline{INTA}$ is active
B. HOLD is active
C. READY is inactive
D. None of the above

gate2002 co-and-architecture interrupts normal

1.14.5 Interrupts: GATE2005-69

https://gateoverflow.in/1392

A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4μsec. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program-controlled mode?

A. 15 B. 25 C. 35 D. 45

gate2005 co-and-architecture interrupts

1.14.6 Interrupts: GATE2009-8, UGCNET-June2012-III-58

https://gateoverflow.in/1300

A CPU generally handles an interrupt by executing an interrupt service routine:

A. As soon as an interrupt is raised.
B. By checking the interrupt register at the end of fetch cycle.
C. By checking the interrupt register after finishing the execution of the current instruction.
D. By checking the interrupt register at fixed time intervals.

gate2009 co-and-architecture interrupts normal ugcnetjune2012iii

1.15 Io Handling (6)

1.15.1 Io Handling: GATE1987-2a

https://gateoverflow.in/80572

State whether the following statements are TRUE or FALSE

In a microprocessor-based system, if a bus (DMA) request and an interrupt request arrive sumultaneously, the microprocessor attends first to the bus request.

gate1987 co-and-architecture interrupts io-handling

1.15.2 Io Handling: GATE1990-4-ii

https://gateoverflow.in/85390

State whether the following statements are TRUE or FALSE with reason:

The data transfer between memory and I/O devices using programmed I/O is faster than interrupt-driven I/O.

gate1990 true-false co-and-architecture io-handling interrupts

1.15.3 Io Handling: GATE1996-1.24

https://gateoverflow.in/2728

For the daisy chain scheme of connecting I/O devices, which of the following statements is true?

A. It gives non-uniform priority to various devices
B. It gives uniform priority to all devices
C. It is only useful for connecting slow devices to a processor device
D. It requires a separate interrupt pin on the processor for each device

gate1996 co-and-architecture io-handling normal

1.15.4 Io Handling: GATE1996-25

https://gateoverflow.in/2777

A hard disk is connected to a 50 MHz processor through a DMA controller. Assume that the initial set-up of a DMA transfer takes 1000 clock cycles for the processor, and assume that the handling of the interrupt at DMA completion requires 500 clock cycles for the processor. The hard disk has a transfer rate of 2000 Kbytes/sec and average block transferred is 4 K bytes. What fraction of the processor time is consumed by the disk, if the disk is actively transferring 100% of the time?

gate1996 co-and-architecture io-handling dma normal

1.15.5 Io Handling: GATE1997-2.4

https://gateoverflow.in/2230

The correct matching for the following pairs is:

(A) DMA I/O	(1) High speed RAM
(B) Cache	(2) Disk
(C) Interrupt I/O	(3) Printer
(D) Condition Code Register	(4) ALU

A. $A-4 \quad B-3 \quad C-1 \quad D-2$
B. $A-2 \quad B-1 \quad C-3 \quad D-4$
C. $A-4 \quad B-3 \quad C-2 \quad D-1$
D. $A-2 \quad B-3 \quad C-4 \quad D-1$

gate1997 co-and-architecture normal io-handling

1.15.6 Io Handling: GATE2008-64, ISRO2009-13

https://gateoverflow.in/487

Which of the following statements about synchronous and asynchronous I/O is NOT true?

A. An ISR is invoked on completion of I/O in synchronous I/O but not in asynchronous I/O
B. In both synchronous and asynchronous I/O, an ISR (Interrupt Service Routine) is invoked after completion of the I/O
C. A process making a synchronous I/O call waits until I/O is complete, but a process making an asynchronous I/O call does not wait for completion of the I/O
D. In the case of synchronous I/O, the process waiting for the completion of I/O is woken up by the ISR that is invoked after the completion of I/O

gate2008 operating-system io-handling normal isro2009

1.16 Machine Instructions (18)

1.16.1 Machine Instructions: GATE1988-9i

https://gateoverflow.in/94384

The following program fragment was written in an assembly language for a single address computer with one accumulator register:

```
LOAD B
MULT C
STORE T1
ADD A
STORE T2
MULT T2
ADD T1
STORE Z
```

Give the arithmetic expression implemented by the fragment.

gate1988 normal descriptive co-and-architecture machine-instructions

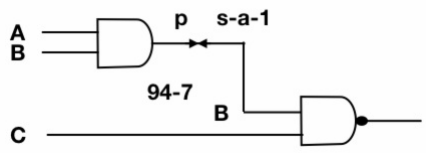
1.16.2 Machine Instructions: GATE1994-12

https://gateoverflow.in/2508

a. Assume that a CPU has only two registers R_1 and R_2 and that only the following instruction is available $XOR\, R_i, R_j; \{R_j \leftarrow R_i \oplus R_j, \text{ for } i, j = 1, 2\}$

   Using this XOR instruction, find an instruction sequence in order to exchange the contents of the registers R_1 and R_2

b. The line p of the circuit shown in figure has stuck at 1 fault. Determine an input test to detect the fault.



gate1994 co-and-architecture machine-instructions normal

1.16.3 Machine Instructions: GATE1999-17

https://gateoverflow.in/1516

Consider the following program fragment in the assembly language of a certain hypothetical processor. The processor has three general purpose registers $R1, R2$and $R3$. The meanings of the instructions are shown by comments (starting with ;) after the instructions.

```
X:  CMP R1, 0;  Compare R1 and 0, set flags appropriately in status register
    JZ  Z;   Jump if zero to target Z
    MOV R2, R1; Copy contents of R1 to R2
    SHR R1; Shift right R1 by 1 bit
    SHL R1; Shift left R1 by 1 bit
    CMP R2, R1; Compare R2 and R1 and set flag in status register
    JZ  Y;    Jump if zero to target Y
    INC R3; Increment R3 by 1;
Y:  SHR R1; Shift right R1 by 1 bit
    JMP X;  Jump to target X
Z:...
```

A. Initially $R1, R2$ and $R3$ contain the values 5,0 and 0 respectively, what are the final values of $R1$ and $R3$ when control reaches Z?

B. In general, if $R1, R2$ and $R3$ initially contain the values n, 0, and 0 respectively. What is the final value of $R3$ when control reaches Z?

gate1999 co-and-architecture machine-instructions normal

1.16.4 Machine Instructions: GATE2003-48

https://gateoverflow.in/938

Consider the following assembly language program for a hypothetical processor A, B, and C are $8-$bit registers. The meanings of various instructions are shown as comments.

	MOV B, #0	;	$B \leftarrow 0$
	MOV C, #8	;	$C \leftarrow 8$
Z:	CMP C, #0	;	compare C with 0
	JZ X	;	jump to X if zero flag is set
	SUB C, #1	;	$C \leftarrow C - 1$
	RRC A, #1	;	right rotate A through carry by one bit. Thus:
		;	If the initial values of A and the carry flag are $a_7 \ldots a_0$ and
		;	c_0 respectively, their values after the execution of this
		;	instruction will be $c_0 a_7 \ldots a_1$ and a_0 respectively.
	JC Y	;	jump to Y if carry flag is set
	JMP Z	;	jump to Z
Y:	ADD B, #1	;	$B \leftarrow B + 1$
	JMP Z	;	jump to Z
X:		;	

If the initial value of register A is A0 the value of register B after the program execution will be

A. the number of 0 bits in A_0
B. the number of 1 bits in A_0
C. A_0
D. 8

gate2003 co-and-architecture machine-instructions normal

1.16.5 Machine Instructions: GATE2003-49

https://gateoverflow.in/43577

Consider the following assembly language program for a hypothetical processor A, B, and C are 8 bit registers. The meanings of various instructions are shown as comments.

```
        MOV B, #0 ; B ← 0
        MOV C, #8 ; C ← 8
Z:      CMP C, #0 ; compare C with 0
        JZ X      ; jump to X if zero flag is set
        SUB C, #1 ; C ← C − 1
        RRC A, #1 ; right rotate A through carry by one bit. Thus:
                  ; If the initial values of A and the carry flag are a7..a0 and
                  ; c0 respectively, their values after the execution of this
                  ; instruction will be c0 a7..a1 and a0 respectively.
        JC Y      ; jump to Y if carry flag is set
        JMP Z     ; jump to Z

Y:      ADD B, #1 ; B ← B + 1
        JMP Z     ; jump to Z
X:
```

Which of the following instructions when inserted at location X will ensure that the value of the register A after program execution is as same as its initial value?

A. RRC A, #1
B. NOP ; no operation
C. LRC A, #1; left rotate A through carry flag by one bit
D. ADD A, #1

gate2003 co-and-architecture machine-instructions normal

1.16.6 Machine Instructions: GATE2004-63

https://gateoverflow.in/1058

Consider the following program segment for a hypothetical CPU having three user registers R_1, R_2 and R_3.

Instruction	Operation	Instruction size (in words)
MOV $R_1, 5000$	$R_1 \leftarrow \text{Memory}[5000]$	2
MOV $R2(R1)$	$R2 \leftarrow \text{Memory}[(R_1)]$	1
ADD R_2, R_3	$R2 \leftarrow R_2 + R_3$	1
MOV $6000, R_2$	$\text{Memory}[6000] \leftarrow R_2$	2
HALT	Machine Halts	1

Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be

A. 1007 B. 1020 C. 1024 D. 1028

gate2004 co-and-architecture machine-instructions normal

1.16.7 Machine Instructions: GATE2004-64

https://gateoverflow.in/43570

Consider the following program segment for a hypothetical CPU having three user registers R_1, R_2 and R_3.

Instruction	Operation	Instruction size (in Words)
MOV $R_1, 5000$	$R1 \leftarrow \text{Memory}[5000]$	2
MOV $R_2(R_1)$	$R2 \leftarrow \text{Memory}[(R_1)]$	1
ADD R_2, R_3	$R_2 \leftarrow R_2 + R_3$	1
MOV $6000, R_2$	$\text{Memory}[6000] \leftarrow R_2$	2
Halt	Machine Halts	1

Let the clock cycles required for various operations be as follows:

Register to/from memory transfer	3 clock cycles
ADD with both operands in register	1 clock cycles
Instruction fetch and decode	2 clock cycles

The total number of clock cycles required to execute the program is

A. 29 B. 24 C. 23 D. 20

gate2004 co-and-architecture machine-instructions normal

1.16.8 Machine Instructions: GATE2004-IT-46

https://gateoverflow.in/3689

If we use internal data forwarding to speed up the performance of a CPU (R1, R2 and R3 are registers and M[100] is a memory reference), then the sequence of operations

R1 → M[100]
M[100] → R2
M[100] → R3

can be replaced by

A. R1 → R3
R2 → M[100]

B. M[100] → R2
R1 → R2
R1 → R3

C. R1 → M[100]
R2 → R3

D. R1 → R2
R1 → R3
R1 → M[100]

gate2004-it co-and-architecture machine-instructions easy

1.16.9 Machine Instructions: GATE2006-09, ISRO2009-35

https://gateoverflow.in/888

A CPU has 24-*bit* instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

A. 400 B. 500 C. 600 D. 700

gate2006 co-and-architecture machine-instructions easy isro2009

1.16.10 Machine Instructions: GATE2007-54

https://gateoverflow.in/1252

In a simplified computer the instructions are:

OP R_j, R_i	Perform R_jOP R_i and store the result in register R_j
OP m, R_i	Perform val OP R_i and store the result in register R_i val denotes the content of the memory location m
MOV m, R_i	Moves the content of memory location m to register R_i
MOV R_i, m	Moves the content of register R_i to memory location m

The computer has only two registers, and OP is either ADD or SUB. Consider the following basic block:

- $t_1 = a + b$
- $t_2 = c + d$
- $t_3 = e - t_2$
- $t_4 = t_1 - t_3$

Assume that all operands are initially in memory. The final value of the computation should be in memory. What is the minimum number of MOV instructions in the code generated for this basic block?

A. 2 B. 3 C. 5 D. 6

gate2007 co-and-architecture machine-instructions normal

1.16.11 Machine Instructions: GATE2007-71

https://gateoverflow.in/1269

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	R1← M[3000]	2
LOOP:	MOV R2,(R3)	R2← M[R3]	1
	ADD R2,R1	R2← R1 + R2	1
	MOV (R3),R2	M[R3]← R2	1
	INC R3	R3← R3 + 1	1
	DEC R1	R1← R1 – 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

A. 10 B. 11 C. 20 D. 21

gate2007 co-and-architecture machine-instructions interrupts normal

1.16.12 Machine Instructions: GATE2007-72

https://gateoverflow.in/43515

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	R1← M[3000]	2
LOOP:	MOV R2,(R3)	R2← M[R3]	1
	ADD R2,R1	R2← R1 + R2	1
	MOV (R3),R2	M[R3]← R2	1
	INC R3	R3← R3 + 1	1
	DEC R1	R1← R1 – 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:

A. 100 B. 101 C. 102 D. 110

gate2007 co-and-architecture machine-instructions interrupts normal

1.16.13 Machine Instructions: GATE2007-73

https://gateoverflow.in/43516

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	R1← M[3000]	2
LOOP:	MOV R2,(R3)	R2← M[R3]	1
	ADD R2,R1	R2← R1 + R2	1
	MOV (R3),R2	M[R3]← R2	1
	INC R3	R3← R3 + 1	1
	DEC R1	R1← R1 – 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction “INC R3”, what return address will be pushed on to the stack?

A. 1005 B. 1020 C. 1024 D. 1040

gate2007 co-and-architecture machine-instructions interrupts normal

1.16.14 Machine Instructions: GATE2007-IT-41

https://gateoverflow.in/3476

Following table indicates the latencies of operations between the instruction producing the result and instruction using the result.

Instruction producing the result	Instruction using the result	Latency
ALU Operation	ALU Operation	2
ALU Operation	Store	2
Load	ALU Operation	1
Load	Store	0

Consider the following code segment:

```
Load R1, Loc 1; Load R1 from memory location Loc1
Load R2, Loc 2; Load R2 from memory location Loc 2
Add R1, R2, R1; Add R1 and R2 and save result in R1
Dec R2;         Decrement R2
Dec R1;         Decrement R1
Mpy R1, R2, R3; Multiply R1 and R2 and save result in R3
Store R3, Loc 3; Store R3 in memory location Loc 3
```

What is the number of cycles needed to execute the above code segment assuming each instruction takes one cycle to execute?

A. 7 B. 10 C. 13 D. 14

gate2007-it co-and-architecture machine-instructions normal

1.16.15 Machine Instructions: GATE2008-34

https://gateoverflow.in/445

Which of the following must be true for the RFE (Return From Exception) instruction on a general purpose processor?

I. It must be a trap instruction
II. It must be a privileged instruction
III. An exception cannot be allowed to occur during execution of an RFE instruction

A. I only B. II only C. I and II only D. I, II and III only

gate2008 co-and-architecture machine-instructions normal

1.16.16 Machine Instructions: GATE2008-IT-38

https://gateoverflow.in/3348

Assume that EA = (X)+ is the effective address equal to the contents of location X, with X incremented by one word length after the effective address is calculated; EA = −(X) is the effective address equal to the contents of location X, with X decremented by one word length before the effective address is calculated; EA = (X)− is the effective address equal to the contents of location X, with X decremented by one word length after the effective address is calculated. The format of the instruction is (opcode, source, destination), which means (destination ← source op destination). Using X as a stack pointer, which of the following instructions can pop the top two elements from the stack, perform the addition operation and push the result back to the stack.

A. ADD (X)−, (X)
B. ADD (X), (X)−
C. ADD −(X), (X)+
D. ADD −(X), (X)

gate2008-it co-and-architecture machine-instructions normal

1.16.17 Machine Instructions: GATE2015-2-42

https://gateoverflow.in/8215

Consider a processor with byte-addressable memory. Assume that all registers, including program counter (PC) and Program Status Word (PSW), are size of two bytes. A stack in the main memory is implemented from memory location $(0100)_{16}$ and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is $(016E)_{16}$. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

- Store the current value of PC in the stack
- Store the value of PSW register in the stack
- Load the statring address of the subroutine in PC

So now the value of SP = (016E)16 + 4 = (0172)16 after execute CALL instruction..

The content of PC just before the fetch of a CALL instruction is $(5FA0)_{16}$. After execution of the CALL instruction, the value of the stack pointer is:

A. $(016A)_{16}$ B. $(016C)_{16}$ C. $(0170)_{16}$ D. $(0172)_{16}$

gate2015-2 co-and-architecture machine-instructions easy

1.16.18 Machine Instructions: GATE2016-2-10

https://gateoverflow.in/39547

A processor has 40 distinct instruction and 24 general purpose registers. A 32-bit instruction word has an opcode, two registers operands and an immediate operand. The number of bits available for the immediate operand field is_____.

gate2016-2 machine-instructions co-and-architecture easy numerical-answers

1.17 Memory Interfacing (2)

1.17.1 Memory Interfacing: GATE2016-1-09

https://gateoverflow.in/39632

A processor can support a maximum memory of $4GB$, where the memory is word-addressable (a word consists of two bytes). The size of address bus of the processor is at least _____bits.

gate2016-1 co-and-architecture easy numerical-answers memory-interfacing

1.17.2 Memory Interfacing: GATE2018-23

https://gateoverflow.in/204097

A $32\text{-}bit$ wide main memory unit with a capacity of $1\ GB$ is built using $256\ M \times 4 - bit$ DRAM chips. The number of rows of memory cells in the DRAM chip is 2^{14}. The time taken to perform one refresh operation is $50\ nanoseconds$. The refresh period is 2 milliseconds. The percentage (rounded to the closest integer) of the time available for performing the memory read/write operations in the main memory unit is_____.

Time spent in refresh =Total time to Refresh all Rows Refresh period*100
=0.8192ms2.0ms*100 =40.96%
Time spent in Read/Write =100−40.96=59.04

gate2018 co-and-architecture memory-interfacing normal numerical-answers

1.18 Microprogramming (13)

1.18.1 Microprogramming: GATE1987-4a

https://gateoverflow.in/81359

Find out the width of the control memory of a horizontal microprogrammed control unit, given the following specifications:

- 16 control lines for the processor consisting of ALU and 7 registers.

- Conditional branching facility by checking 4 status bits.
- Provision to hold 128 words in the control memory.

gate1987 co-and-architecture microprogramming

1.18.2 Microprogramming: GATE1990-8a

https://gateoverflow.in/85669

A single bus CPU consists of four general purpose register, namely, $R0 \ldots\ldots R3, ALU, MAR, MDR, PC, SP$ and IR (Instruction Register). Assuming suitable microinstructions, write a microroutine for the instruction,

$ADDR0, R1$

gate1990 descriptive co-and-architecture microprogramming

1.18.3 Microprogramming: GATE1996-2.25

https://gateoverflow.in/2754

A micro program control unit is required to generate a total of 25 control signals. Assume that during any micro instruction, at most two control signals are active. Minimum number of bits required in the control word to generate the required control signals will be:

A. 2 B. 2.5 C. 10 D. 12

gate1996 co-and-architecture microprogramming normal

1.18.4 Microprogramming: GATE1997-5.3

https://gateoverflow.in/2254

A micro instruction is to be designed to specify:

a. none or one of the three micro operations of one kind and
b. none or upto six micro operations of another kind

The minimum number of bits in the micro-instruction is:

A. 9 B. 5 C. 8 D. None of the above

gate1997 co-and-architecture microprogramming normal

1.18.5 Microprogramming: GATE1999-2.19

https://gateoverflow.in/1497

Arrange the following configuration for CPU in decreasing order of operating speeds:
Hard wired control, Vertical microprogramming, Horizontal microprogramming.

A. Hard wired control, Vertical microprogramming, Horizontal microprogramming.
B. Hard wired control, Horizontal microprogramming, Vertical microprogramming.
C. Horizontal microprogramming, Vertical microprogramming, Hard wired control.
D. Vertical microprogramming, Horizontal microprogramming, Hard wired control.

gate1999 co-and-architecture microprogramming normal

1.18.6 Microprogramming: GATE2002-2.7

https://gateoverflow.in/837

Horizontal microprogramming:

A. does not require use of signal decoders
B. results in larger sized microinstructions than vertical microprogramming
C. uses one bit for each control signal
D. all of the above

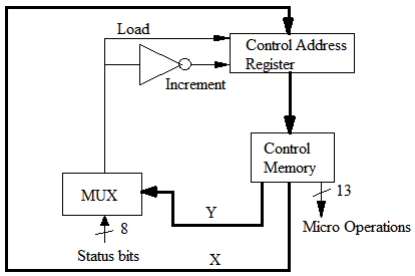
gate2002 co-and-architecture microprogramming

1.18.7 Microprogramming: GATE2004-67

https://gateoverflow.in/1061

The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y).

There are 8 status bits in the input of the MUX.



How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

A. $10, 3, 1024$ B. $8, 5, 256$ C. $5, 8, 2048$ D. $10, 3, 512$

gate2004 co-and-architecture microprogramming normal

1.18.8 Microprogramming: GATE2004-IT-49

https://gateoverflow.in/3692

A CPU has only three instructions $I1, I2$ and $I3$, which use the following signals in time steps $T1 - T5$:

$I1$: $T1$: Ain, Bout, Cin
$T2$: PCout, Bin
$T3$: Zout, Ain
$T4$: Bin, Cout
$T5$: End

$I2$: $T1$: Cin, Bout, Din
$T2$: Aout, Bin
$T3$: Zout, Ain
$T4$: Bin, Cout
$T5$: End

$I3$: $T1$: Din, Aout
$T2$: Ain, Bout
$T3$: Zout, Ain
$T4$: Dout, Ain
$T5$: End

Which of the following logic functions will generate the hardwired control for the signal Ain ?

A. $T1.I1 + T2.I3 + T4.I3 + T3$ B. $(T1 + T2 + T3).I3 + T1.I1$
C. $(T1 + T2).I1 + (T2 + T4).I3 + T3$ D. $(T1 + T2).I2 + (T1 + T3).I1 + T3$

gate2004-it co-and-architecture microprogramming normal

1.18.9 Microprogramming: GATE2005-IT-45

https://gateoverflow.in/3806

A hardwired CPU uses 10 control signals S_1 to S_{10}, in various time steps T_1 to T_5, to implement 4 instructions I_1 to I_4 as shown below:

	$\mathbf{T_1}$	$\mathbf{T_2}$	$\mathbf{T_3}$	$\mathbf{T_4}$	$\mathbf{T_5}$
$\mathbf{I_1}$	S_1, S_3, S_5	S_2, S_4, S_6	S_1, S_7	S_{10}	S_3, S_8
$\mathbf{I_2}$	S_1, S_3, S_5	S_8, S_9, S_{10}	$S_5, S_6 S_7$	S_6	S_{10}
$\mathbf{I_3}$	S_1, S_3, S_5	S_7, S_8, S_{10}	S_2, S_6, S_9	S_{10}	S_1, S_3
$\mathbf{I_4}$	S_1, S_3, S_5	S_2, S_6, S_7	S_5, S_{10}	S_6, S_9	S_{10}

Which of the following pairs of expressions represent the circuit for generating control signals S_5 and S_{10} respectively?
($(I_j + I_k)T_n$ indicates that the control signal should be generated in time step T_n if the instruction being executed is I_j or l_k)

A. $S_5 = T_1 + I_2 \cdot T_3$ and
$S_{10} = (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$
B. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and
$S_{10} = (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$
C. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and

$S_{10} = (I_2 + I_3 + I_4) \cdot T_2 + (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$

D. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and
$S_{10} = (I_2 + I_3) \cdot T_2 + I_4 \cdot T_3 + (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$

gate2005-it co-and-architecture microprogramming normal

1.18.10 Microprogramming: GATE2005-IT-49

https://gateoverflow.in/3810

An instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows:

Group 1 : 20 signals, Group 2 : 70 signals, Group 3 : 2 signals, Group 4 : 10 signals, Group 5 : 23 signals.

How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming?

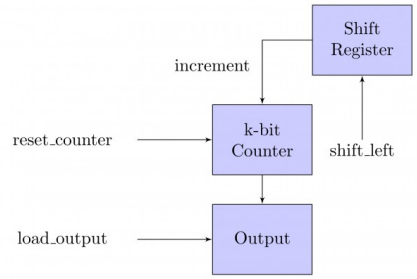
A. 0 B. 103 C. 22 D. 55

gate2005-it co-and-architecture microprogramming normal

1.18.11 Microprogramming: GATE2006-IT-41

https://gateoverflow.in/3584

The data path shown in the figure computes the number of $1s$ in the $32 - bit$ input word corresponding to an unsigned even integer stored in the shift register.
The unsigned counter, initially zero, is incremented if the most significant bit of the shift register is 1.



The microprogram for the control is shown in the table below with missing control words for microinstructions $I_1, I_2, \ldots I_n$.

Microinstruction	Reset_Counter	Shift_left	Load_output
BEGIN	1	0	0
I1	?	?	?
:	:	:	:
In	?	?	?
END	0	0	1

The counter width (k), the number of missing microinstructions (n), and the control word for microinstructions $I_1, I_2, \ldots I_n$ are, respectively,

A. $32, 5, 010$ B. $5, 32, 010$ C. $5, 31, 011$ D. $5, 31, 010$

gate2006-it co-and-architecture microprogramming normal

1.18.12 Microprogramming: GATE2008-IT-39

https://gateoverflow.in/3349

Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal microprogrammed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

A. $125, 7$ B. $125, 10$ C. $135, 9$ D. $135, 10$

Since it is horizontal for control word, 125 control signals+10 bits =135 bits will be required.

gate2008-it co-and-architecture microprogramming normal

1.18.13 Microprogramming: GATE2013-28

https://gateoverflow.in/1539

Consider the following sequence of micro-operations.

```
MBR ← PC   MAR ← X   PC ← Y   Memory ← MBR
```

Which one of the following is a possible operation performed by this sequence?

A. Instruction fetch
B. Operand fetch
C. Conditional branch
D. Initiation of interrupt service

gate2013 co-and-architecture microprogramming normal

1.19 Pipelining (34)

1.19.1 Pipelining: GATE1999-13

https://gateoverflow.in/1512

An instruction pipeline consists of 4 stages – Fetch (F), Decode field (D), Execute (E) and Result Write (W). The 5 instructions in a certain instruction sequence need these stages for the different number of clock cycles as shown by the table below

	No. of cycles needed for			
Instruction	**F**	**D**	**E**	**W**
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1
5	1	2	1	2

Instruction	F	D	E	W
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1
5	1	2	1	2

Find the number of clock cycles needed to perform the 5 instructions.

gate1999 co-and-architecture pipelining normal

1.19.2 Pipelining: GATE2000-1.8

https://gateoverflow.in/631

Comparing the time T1 taken for a single instruction on a pipelined CPU with time T2 taken on a non-pipelined but identical CPU, we can say that

A. $T1 \leq T2$
B. $T1 \geq T2$
C. $T1 < T2$
D. T1 and T2 plus the time taken for one instruction fetch cycle

gate2000 pipelining co-and-architecture easy

1.19.3 Pipelining: GATE2000-12

https://gateoverflow.in/683

An instruction pipeline has five stages where each stage take 2 nanoseconds and all instruction use all five stages. Branch instructions are not overlapped. i.e., the instruction after the branch is not fetched till the branch instruction is completed. Under ideal conditions,

A. Calculate the average instruction execution time assuming that 20% of all instructions executed are branch instruction. Ignore the fact that some branch instructions may be conditional.
B. If a branch instruction is a conditional branch instruction, the branch need not be taken. If the branch is not taken, the following instructions can be overlapped. When 80% of all branch instructions are conditional branch instructions, and 50% of the conditional branch instructions are such that the branch is taken, calculate the average instruction execution time.

gate2000 co-and-architecture pipelining normal descriptive

1.19.4 Pipelining: GATE2001-12

https://gateoverflow.in/753

Consider a $5-$stage pipeline - IF (Instruction Fetch), ID (Instruction Decode and register read), EX (Execute), MEM (memory), and WB (Write Back). All (memory or register) reads take place in the second phase of a clock cycle and all writes occur in the first phase. Consider the execution of the following instruction sequence:

I1:	sub $r2, r3, r4$	$/* \quad r2 \leftarrow r3 - r4 \quad */$
I2:	sub $r4, r2, r3$	$/* \quad r4 \leftarrow r2 - r3 \quad */$
I3:	sw $r2, 100(r1)$	$/* \quad M[r1 + 100] \leftarrow \text{r2} \quad */$
I4:	sub $r3, r4, r2$	$/* \quad r3 \leftarrow r4 - r2 \quad */$

A. Show all data dependencies between the four instructions.
B. Identify the data hazards.
C. Can all hazards be avoided by forwarding in this case.

gate2001 co-and-architecture pipelining normal descriptive

1.19.5 Pipelining: GATE2002-2.6, ISRO2008-19

https://gateoverflow.in/836

The performance of a pipelined processor suffers if:

A. the pipeline stages have different delays
B. consecutive instructions are dependent on each other
C. the pipeline stages share hardware resources
D. All of the above

gate2002 co-and-architecture pipelining easy isro2008

1.19.6 Pipelining: GATE2003-10, ISRO-DEC2017-41

https://gateoverflow.in/901

For a pipelined CPU with a single ALU, consider the following situations

I. The $j + 1^{st}$ instruction uses the result of the j^{th} instruction as an operand
II. The execution of a conditional jump instruction
III. The j^{th} and $j + 1^{st}$ instructions require the ALU at the same time.

Which of the above can cause a hazard

A. I and II only B. II and III only C. III only D. All the three

gate2003 co-and-architecture pipelining normal isrodec2017

1.19.7 Pipelining: GATE2004-69

https://gateoverflow.in/1063

A 4-stage pipeline has the stage delays as $150, 120, 160$ and 140 $nanoseconds$, respectively. Registers that are used between the stages have a delay of 5 $nanoseconds$ each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be:

A. 120.4 microseconds
B. 160.5 microseconds
C. 165.5 microseconds
D. 590.0 microseconds

gate2004 co-and-architecture pipelining normal

1.19.8 Pipelining: GATE2004-IT-47

https://gateoverflow.in/3690

Consider a pipeline processor with 4 stages $S1$ to $S4$. We want to execute the following loop:

```
for (i = 1; i < = 1000; i++)
    {I1, I2, I3, I4}
```

where the time taken (in ns) by instructions $I1$ to $I4$ for stages $S1$ to $S4$ are given below:

	S_1	S_2	S_3	S_4
I1	1	2	1	2
I2	2	1	2	1
I3	1	1	2	1
I4	2	1	2	1

The output of $I1$ for $i = 2$ will be available after

A. 11 ns B. 12 ns C. 13 ns D. 28 ns

gate2004-it co-and-architecture pipelining normal

1.19.9 Pipelining: GATE2005-68

https://gateoverflow.in/1391

A 5 stage pipelined CPU has the following sequence of stages:

- IF – instruction fetch from instruction memory
- RD – Instruction decode and register read
- EX – Execute: ALU operation for data and address computation
- MA – Data memory access – for write access, the register read at RD state is used.
- WB – Register write back

Consider the following sequence of instructions:

- I_1: L $R0$, loc 1; $R0 <= M[loc1]$
- I_2: A $R0$, $R0$; $R0 <= R0 + R0$
- I_3: S $R2$, $R0$; $R2 <= R2 - R0$

Let each stage take one clock cycle.

What is the number of clock cycles taken to complete the above sequence of instructions starting from the fetch of I_1?

A. 8 B. 10 C. 12 D. 15

gate2005 co-and-architecture pipelining normal

1.19.10 Pipelining: GATE2005-IT-44

https://gateoverflow.in/3805

We have two designs $D1$ and $D2$ for a synchronous pipeline processor. $D1$ has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design $D2$ has 8 pipeline stages each with 2 nsec execution time How much time can be saved using design $D2$ over design $D1$ for executing 100 instructions?

A. 214 nsec B. 202 nsec
C. 86 nsec D. -200 nsec

gate2005-it co-and-architecture pipelining normal

1.19.11 Pipelining: GATE2006-42

https://gateoverflow.in/1818

A CPU has a five-stage pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 109 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, the total execution time of the program is:

A. 1.0 second B. 1.2 seconds C. 1.4 seconds D. 1.6 seconds

gate2006 co-and-architecture pipelining normal

1.19.12 Pipelining: GATE2006-IT-78

https://gateoverflow.in/3622

A pipelined processor uses a $4-$stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement $X = (S - R * (P + Q))/T$ is given below. The values of variables P, Q, R, S and T are available in the registers $R0, R1, R2, R3$ and $R4$ respectively, before the execution of the instruction sequence.

```
ADD     R5, R0, R1      ; R5 ← R0 + R1
MUL     R6, R2, R5      ; R6 ← R2 * R5
SUB     R5, R3, R6      ; R5 ← R3 - R6
DIV     R6, R5, R4      ; R6 ← R5/R4
STORE   R6, X           ; X  ← R6
```

The number of Read-After-Write (RAW) dependencies, Write-After-Read(WAR) dependencies, and Write-After-Write (WAW) dependencies in the sequence of instructions are, respectively,

A. $2, 2, 4$ B. $3, 2, 3$ C. $4, 2, 2$ D. $3, 3, 2$

gate2006-it co-and-architecture pipelining normal

1.19.13 Pipelining: GATE2006-IT-79

https://gateoverflow.in/3623

A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement $X = (S - R * (P + Q))/T$ is given below. The values of variables P, Q, R, S and T are available in the registers $R0, R1, R2, R3$ and $R4$ respectively, before the execution of the instruction sequence.

```
ADD     R5, R0, R1      ; R5 ← R0 + R1
MUL     R6, R2, R5      ; R6 ← R2 * R5
SUB     R5, R3, R6      ; R5 ← R3 -R6
DIV     R6, R5, R4      ; R6 ← R5/R4
STORE   R6, X           ; X ← R6
```

The IF, ID and WB stages take 1 clock cycle each. The EX stage takes 1 clock cycle each for the ADD, SUB and STORE operations, and 3 clock cycles each for MUL and DIV operations. Operand forwarding from the EX stage to the ID stage is used. The number of clock cycles required to complete the sequence of instructions is

A. 10 B. 12 C. 14 D. 16

gate2006-it co-and-architecture pipelining normal

1.19.14 Pipelining: GATE2007-37, ISRO2009-37

https://gateoverflow.in/1235

Consider a pipelined processor with the following four stages:

- IF: Instruction Fetch
- ID: Instruction Decode and Operand Fetch
- EX: Execute
- WB: Write Back

The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

```
ADD     R2, R1, R0      R2 ← R1+R0
MUL     R4, R3, R2      R4 ← R3*R2
SUB     R6, R5, R4      R6 ← R5−R4
```

A. 7 B. 8 C. 10 D. 14

gate2007 co-and-architecture pipelining normal isro2009

1.19.15 Pipelining: GATE2007-IT-6, ISRO2011-25

https://gateoverflow.in/3437

A processor takes 12 cycles to complete an instruction I. The corresponding pipelined processor uses 6 stages with the execution times of $3, 2, 5, 4, 6$ and 2 cycles respectively. What is the asymptotic speedup assuming that a very large number of instructions are to be executed?

A. 1.83 B. 2 C. 3 D. 6

gate2007-it co-and-architecture pipelining normal isro2011

1.19.16 Pipelining: GATE2008-36

https://gateoverflow.in/447

Which of the following are NOT true in a pipelined processor?

I. Bypassing can handle all RAW hazards
II. Register renaming can eliminate all register carried WAR hazards
III. Control hazard penalties can be eliminated by dynamic branch prediction

A. I and II only B. I and III only C. II and III only D. I, II and III

gate2008 pipelining co-and-architecture normal

1.19.17 Pipelining: GATE2008-76

https://gateoverflow.in/496

Delayed branching can help in the handling of control hazards

For all delayed conditional branch instructions, irrespective of whether the condition evaluates to true or false,

A. The instruction following the conditional branch instruction in memory is executed
B. The first instruction in the fall through path is executed
C. The first instruction in the taken path is executed
D. The branch takes longer to execute than any other instruction

gate2008 co-and-architecture pipelining normal

1.19.18 Pipelining: GATE2008-77

https://gateoverflow.in/43487

Delayed branching can help in the handling of control hazards

The following code is to run on a pipelined processor with one branch delay slot:

I1: ADD $R2 \leftarrow R7 + R8$

I2: Sub $R4 \leftarrow R5 - R6$

I3: ADD $R1 \leftarrow R2 + R3$

I4: STORE Memory $[R4] \leftarrow R1$

BRANCH to Label if $R1 == 0$

Which of the instructions I1, I2, I3 or I4 can legitimately occupy the delay slot without any program modification?

A. I1 B. I2 C. I3 D. I4

gate2008 co-and-architecture pipelining normal

1.19.19 Pipelining: GATE2008-IT-40

https://gateoverflow.in/3350

A non pipelined single cycle processor operating at $100\ MHz$ is converted into a synchronous pipelined processor with five stages requiring $2.5\ nsec$, $1.5\ nsec$, $2\ nsec$, $1.5\ nsec$ and $2.5\ nsec$, respectively. The delay of the latches is $0.5\ nsec$. The speedup of the pipeline processor for a large number of instructions is:

A. 4.5 B. 4.0 C. 3.33 D. 3.0

gate2008-it co-and-architecture pipelining normal

1.19.20 Pipelining: GATE2009-28

https://gateoverflow.in/1314

Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions $I1, I2, I3, I4$ in stages $S1, S2, S3, S4$ is shown below:

	S_1	S_2	S_3	S_4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?
For $(i = 1 \text{ to } 2)$ {I1; I2; I3; I4;}

A. 16 B. 23 C. 28 D. 30

gate2009 co-and-architecture pipelining normal

1.19.21 Pipelining: GATE2010-33

https://gateoverflow.in/2207

A $5-$stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	Meaning of instruction
t_0: MUL R_2, R_0, R_1	$\mathrm{R_2} \leftarrow \mathrm{R_0} * \mathrm{R_1}$
t_1: DIV R_5, R_3, R_4	$\mathrm{R_5} \leftarrow \mathrm{R_3} \ / \ \mathrm{R_4}$
t_2: ADD R_2, R_5, R_2	$\mathrm{R_2} \leftarrow \mathrm{R_5} + \mathrm{R_2}$
t_3 : SUB $\mathrm{R_5}, \mathrm{R_2}, \mathrm{R_6}$	$\mathrm{R_5} \leftarrow \mathrm{R_2} - \mathrm{R_6}$

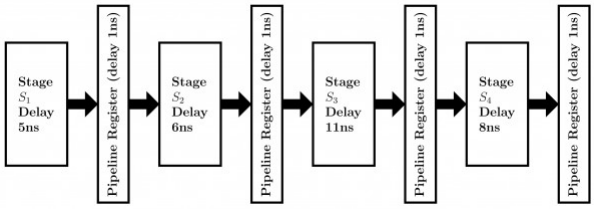
A. 13 B. 15 C. 17 D. 19

gate2010 co-and-architecture pipelining normal

1.19.22 Pipelining: GATE2011-41

https://gateoverflow.in/2143

Consider an instruction pipeline with four stages $(\mathrm{S1}, \mathrm{S2}, \mathrm{S3 \text{ and } S4})$ each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure.



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

A. 4.0 B. 2.5 C. 1.1 D. 3.0

gate2011 co-and-architecture pipelining normal

1.19.23 Pipelining: GATE2012-20, ISRO2016-23

https://gateoverflow.in/52

Register renaming is done in pipelined processors:

A. as an alternative to register allocation at compile time
B. for efficient access to function parameters and local variables
C. to handle certain kinds of hazards
D. as part of address translation

gate2012 co-and-architecture pipelining easy isro2016

1.19.24 Pipelining: GATE2013-45

https://gateoverflow.in/330

Consider an instruction pipeline with five stages without any branch prediction:

Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions $I1, I2, I3, \ldots, I12$ is executed in this pipelined processor. Instruction $I4$ is the only branch instruction and its branch target is $I9$. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is

A. 132
B. 165
C. 176
D. 328

gate2013 normal co-and-architecture pipelining

1.19.25 Pipelining: GATE2014-1-43

https://gateoverflow.in/1921

Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instructions incur 2 pipeline stall cycles is _____

Speed up= pipeline depth / (1+#stalls per cycle)

gate2014-1 co-and-architecture pipelining numerical-answers normal

1.19.26 Pipelining: GATE2014-3-43

https://gateoverflow.in/2077

An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register writeback (WB) with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the ID/RF stage into three stages (ID, RF1, RF2) each of latency $2.2/3$ ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds, respectively. The value of P/Q is _____.

gate2014-3 co-and-architecture pipelining numerical-answers normal

1.19.27 Pipelining: GATE2014-3-9

https://gateoverflow.in/2043

Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.

- P1: Four-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.
- P2: Four-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.
- P3: Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.
- P4: Five-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.

Which processor has the highest peak clock frequency?

A. $P1$ B. $P2$ C. $P3$ D. $P4$

gate2014-3 co-and-architecture pipelining normal

1.19.28 Pipelining: GATE2015-1-38

https://gateoverflow.in/8288

Consider a non-pipelined processor with a clock rate of 2.5 GHz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 GHz. Assume that there are no stalls in the pipeline. The speedup achieved in this pipelined processor is_____.

gate2015-1 co-and-architecture pipelining normal numerical-answers

1.19.29 Pipelining: GATE2015-2-44

https://gateoverflow.in/8218

Consider the sequence of machine instruction given below:

```
MUL   R5, R0, R1
DIV   R6, R2, R3
ADD   R7, R5, R6
SUB   R8, R7, R4
```

In the above sequence, $R0$ to $R8$ are general purpose registers. In the instructions shown, the first register shows the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) Instruction Fetch and Decode (IF), (2) Operand Fetch (OF), (3) Perform Operation (PO) and (4) Write back the result (WB). The IF, OF and WB stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage. The number of clock cycles taken for the execution of the above sequence of instruction is _____.

gate2015-2 co-and-architecture pipelining normal numerical-answers

1.19.30 Pipelining: GATE2015-3-51

https://gateoverflow.in/8560

Consider the following reservation table for a pipeline having three stages S_1, S_2 and S_3.

Time $\rightarrow$					
	1	2	3	4	5
S_1	X				X
S_2		X		X	
S_3			X		

31. In first case Clock cycle time =Max Stage Delay=800;
In second case Clock cycle time =Max Stage Delay=600
#Percentage increase in throughput of pipeline =percentage in Clock Frequency
= {(1/600)-(1\800)}/1\800 = 33.33

The minimum average latency (MAL) is _____

gate2015-3 co-and-architecture pipelining difficult numerical-answers

1.19.31 Pipelining: GATE2016-1-32

https://gateoverflow.in/39691

The stage delays in a 4-stage pipeline are $800, 500, 400$ and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionality equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput increase of the pipeline is _____ percent.

gate2016-1 co-and-architecture pipelining normal numerical-answers

1.19.32 Pipelining: GATE2016-2-33

https://gateoverflow.in/39580

Consider a 3 GHz (gigahertz) processor with a three stage pipeline and stage latencies τ_1, τ_2 and τ_3 such that $\tau_1 = \dfrac{3\tau_2}{4} = 2\tau_3$.
If the longest pipeline stage is split into two pipeline stages of equal latency , the new frequency is _____ GHz, ignoring delays in the pipeline registers.

gate2016-2 co-and-architecture pipelining normal numerical-answers

1.19.33 Pipelining: GATE2017-1-50

https://gateoverflow.in/118719

Instruction execution in a processor is divided into 5 stages, *Instruction Fetch* (IF), *Instruction Decode* (ID), *Operand fetch* (OF), *Execute* (EX), and *Write Back* (WB). These stages take **5, 4, 20, 10** and **3 nanoseconds (ns)** respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of **2 ns**. Two pipelined implementation of the processor are contemplated:

i. a naive pipeline implementation (NP) with 5 stages and
ii. an efficient pipeline (EP) where the OF stage is divided into stages OF1 and OF2 with execution times of **12 ns** and **8 ns** respectively.

The speedup (correct to two decimal places) achieved by EP over NP in executing 20 independent instructions with no hazards

is _____ .

gate2017-1 co-and-architecture pipelining normal numerical-answers

1.19.34 Pipelining: GATE2018-50

https://gateoverflow.in/204125

The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards.

The number of clock cycles required for completion of execution of the sequence of instruction is _____.

gate2018 co-and-architecture pipelining numerical-answers

1.20 Runtime Environments (2)

1.20.1 Runtime Environments: GATE2001-1.10, UGCNET-Dec2012-III-36

https://gateoverflow.in/703

Suppose a processor does not have any stack pointer registers, which of the following statements is true?

A. It cannot have subroutine call instruction
B. It cannot have nested subroutines call
C. Interrupts are not possible
D. All subroutine calls and interrupts are possible

gate2001 co-and-architecture normal ugcnetdec2012iii runtime-environments

1.20.2 Runtime Environments: GATE2008-37, ISRO2009-38

https://gateoverflow.in/448

The use of multiple register windows with overlap causes a reduction in the number of memory accesses for:

I. Function locals and parameters
II. Register saves and restores
III. Instruction fetches

A. I only B. II only C. III only D. I, II and III

gate2008 co-and-architecture normal isro2009 runtime-environments

1.21 Speedup (2)

1.21.1 Speedup: GATE2004-IT-50

https://gateoverflow.in/790

In an enhancement of a design of a CPU, the speed of a floating point unit has been increased by 20% and the speed of a fixed point unit has been increased by 10%. What is the overall speedup achieved if the ratio of the number of floating point operations to the number of fixed point operations is $2:3$ and the floating point operation used to take twice the time taken by the fixed point operation in the original design?

A. 1.155 B. 1.185 C. 1.255 D. 1.285

gate2004-it normal co-and-architecture speedup

1.21.2 Speedup: GATE2014-1-55

https://gateoverflow.in/1935

Consider two processors P_1 and P_2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P_2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P_1. If the clock frequency of P_1 is 1GHZ, then the clock frequency of P_2 (in GHz) is _____.

gate2014-1 co-and-architecture numerical-answers normal speedup

1.22 Stall Cycle Per Instrution (1)

1.22.1 Stall Cycle Per Instrution: Gateoverflow Computer architecture 2 exam question https://gateoverflow.in/286401

Suppose there are 500 memory references in which 50 misses in the 1st level cache and 20 misses in the 2nd level cache . Let the miss penalty from L2 cache to memory is 100 cycles . Hit time in L2 cache is 20 cycles and hit time in L1 cache is 10 cycles . If there are 2.5 memory reference/instruction , average number of stall cycles per instruction will be _____

Ans is : 15

Can any explain how to solve this type of question, Thanks in advance.

gateoverflow co-and-architecture stall-cycle-per-instrution

1.23 Virtual Memory (3)

1.23.1 Virtual Memory: GATE1991-03,iii https://gateoverflow.in/517

03. Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:

(iii) The total size of address space in a virtual memory system is limited by:

A. the length of MAR
B. the available secondary storage
C. the available main memory
D. all of the above
E. none of the above

gate1991 co-and-architecture virtual-memory normal

1.23.2 Virtual Memory: GATE2004-47 https://gateoverflow.in/318

Consider a system with a two-level paging scheme in which a regular memory access takes $150\ nanoseconds$, and servicing a page fault takes $8\ milliseconds$. An average instruction takes 100 nanoseconds of CPU time, and two memory accesses. The TLB hit ratio is 90%, and the page fault rate is one in every $10,000$ instructions. What is the effective average instruction execution time?

A. 645 nanoseconds
B. 1050 nanoseconds
C. 1215 nanoseconds
D. 1230 nanoseconds

gate2004 co-and-architecture virtual-memory normal

1.23.3 Virtual Memory: GATE2008-38 https://gateoverflow.in/449

In an instruction execution pipeline, the earliest that the data TLB (Translation Lookaside Buffer) can be accessed is:

A. before effective address calculation has started
B. during effective address calculation
C. after effective address calculation has completed
D. after data cache lookup has completed

gate2008 co-and-architecture virtual-memory normal