4 Digital Logic (267)

Boolean algebra. Combinational and sequential circuits. Minimization. Number representations and computer arithmetic (fixed and floating point)

4.1 Adder (10)

4.1.1 Adder: GATE1988-4ii

https://gateoverflow.in/94360

Using binary full adders and other logic gates (if necessary), design an adder for adding 4-bit number (including sign) in 2's complement notation.

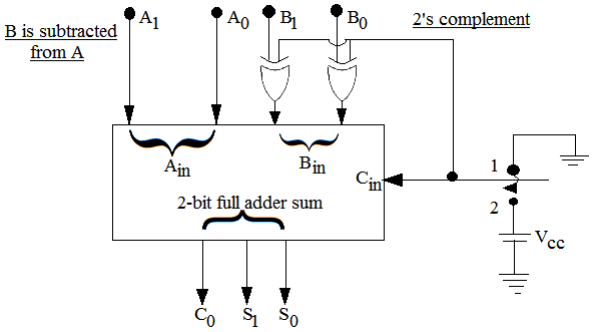
gate1988 digital-logic descriptive adder

4.1.2 Adder: GATE1990-1-i

https://gateoverflow.in/83829

Fill in the blanks:

In the two bit full-adder/subtractor unit shown in below figure, when the switch is in position 2 _____ using _____ arithmetic.



gate1990 digital-logic adder

4.1.3 Adder: GATE1993-9

https://gateoverflow.in/2306

Assume that only half adders are available in your laboratory. Show that any binary function can be implemented using half adders only.

gate1993 digital-logic adder

4.1.4 Adder: GATE1997-2.5

https://gateoverflow.in/2231

An N-bit carry lookahead adder, where N is a multiple of 4, employs ICs 74181 (4 bit ALU) and 74182 (4 bit carry lookahead generator).

The minimum addition time using the best architecture for this adder is

A. proportional to N
B. proportional to $\log N$
C. a constant
D. None of the above

gate1997 digital-logic normal adder

4.1.5 Adder: GATE1999-2.16

https://gateoverflow.in/1494

The number of full and half-adders required to add 16-bit numbers is

A. 8 half-adders, 8 full-adders
B. 1 half-adder, 15 full-adders
C. 16 half-adders, 0 full-adders
D. 4 half-adders, 12 full-adders

OR gate= (n-1)
Half-adder= (2n-1)

gate1999 digital-logic normal adder

4.1.6 Adder: GATE2003-46

https://gateoverflow.in/937

Consider the ALU shown below.

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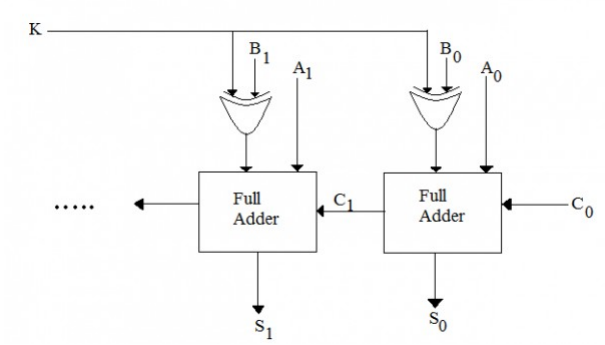

If the operands are in $2's$ complement representation, which of the following operations can be performed by suitably setting the control lines K and C_0 only (+ and – denote addition and subtraction respectively)?

A. $A + B$, and $A - B$, but not $A + 1$
B. $A + B$, and $A + 1$, but not $A - B$
C. $A + B$, but not $A - B$ or $A + 1$
D. $A + B$, and $A - B$, and $A + 1$

gate2003 digital-logic normal adder

4.1.7 Adder: GATE2004-62 https://gateoverflow.in/1057

A 4-bit carry look ahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is one time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.

A. 4 time units
B. 6 time units
C. 10 time units
D. 12 time units

gate2004 digital-logic normal adder

4.1.8 Adder: GATE2015-2-48 https://gateoverflow.in/8250

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit-ripple-carry binary adder is implemented by using four full adders. The total propagation time of this 4-bit binary adder in microseconds is _____.

gate2015-2 digital-logic adder normal numerical-answers

4.1.9 Adder: GATE2016-1-33 https://gateoverflow.in/39688

Consider a carry look ahead adder for adding two n-bit integers, built using gates of fan-in at most two. The time to perform addition using this adder is

A. $\Theta(1)$
B. $\Theta(\log(n))$
C. $\Theta(\sqrt{n})$
D. $\Theta(n))$

gate2016-1 digital-logic adder normal

4.1.10 Adder: GATE2016-2-07 https://gateoverflow.in/39575

Consider an eight-bit ripple-carry adder for computing the sum of A and B, where A and B are integers represented in 2's complement form. If the decimal value of A is one, the decimal value of B that leads to the longest latency for the sum to stabilize is _____

gate2016-2 digital-logic adder normal numerical-answers

4.2 Array Multiplier (2)

4.2.1 Array Multiplier: GATE1999-1.21 https://gateoverflow.in/1474

The maximum gate delay for any output to appear in an array multiplier for multiplying two n bit numbers is

A. $O(n^2)$ B. $O(n)$ C. $O(\log n)$ D. $O(1)$

gate1999 digital-logic normal array-multiplier

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4.2.2 Array Multiplier: GATE2003-11

https://gateoverflow.in/902

Consider an array multiplier for multiplying two n bit numbers. If each gate in the circuit has a unit delay, the total delay of the multiplier is

A. $\Theta(1)$ B. $\Theta(\log n)$ C. $\Theta(n)$ D. $\Theta(n^2)$

gate2003 digital-logic normal array-multiplier

4.3 Binary Codes (2)

4.3.1 Binary Codes: GATE2006-40

https://gateoverflow.in/1816

Consider numbers represented in 4-bit Gray code. Let $h_3h_2h_1h_0$ be the Gray code representation of a number n and let $g_3g_2g_1g_0$ be the Gray code of $(n+1)(modulo16)$ value of the number. Which one of the following functions is correct?

A. $g_0(h_3h_2h_1h_0) = \sum(1,2,3,6,10,13,14,15)$
B. $g_1(h_3h_2h_1h_0) = \sum(4,9,10,11,12,13,14,15)$
C. $g_2(h_3h_2h_1h_0) = \sum(2,4,5,6,7,12,13,15)$
D. $g_3(h_3h_2h_1h_0) = \sum(0,1,6,7,10,11,12,13)$

gate2006 digital-logic number-representation binary-codes normal

4.3.2 Binary Codes: GATE2017-2-34

https://gateoverflow.in/118376

Consider the binary code that consists of only four valid codewords as given below:

00000, 01011, 10101, 11110

Let the minimum Hamming distance of the code p and the maximum number of erroneous bits that can be corrected by the code be q. Then the values of p and q are

Haming distance = min of all hamming distances =3
Now to correct d bit error we need hamming distance = 2d+1

A. $p = 3$ and $q = 1$ B. $p = 3$ and $q = 2$ C. $p = 4$ and $q = 1$ D. $p = 4$ and $q = 2$

gate2017-2 digital-logic binary-codes

4.4 Boolean Algebra (31)

4.4.1 Boolean Algebra: GATE1987-12-a

https://gateoverflow.in/82556

The Boolean expression $A \oplus B \oplus A$ is equivalent to

A. $AB + \bar{A}\bar{B}$ B. $\bar{A}B + A\bar{B}$ C. B D. $\bar{A}$

gate1987 digital-logic boolean-algebra easy

4.4.2 Boolean Algebra: GATE1988-2-iii

https://gateoverflow.in/91679

Let $*$ be defined as a Boolean operation given as $x * y = \bar{x}\bar{y} + xy$ and let $C = A * B$. If $C = 1$ then prove that $A = B$.

gate1988 digital-logic descriptive boolean-algebra

4.4.3 Boolean Algebra: GATE1989-4-x

https://gateoverflow.in/88166

Provide short answers to the following questions:

A switching function is said to be neutral if the number of input combinations for which its value is 1 is equal to the number of input combinations for which its value is 0. Compute the number of neutral switching functions of n variables (for a given n).

gate1989 descriptive digital-logic boolean-algebra

4.4.4 Boolean Algebra: GATE1989-5-a

https://gateoverflow.in/88230

Find values of Boolean variables A, B, C which satisfy the following equations:

- A+ B = 1
- AC = BC
- A + C = 1
- AB = 0

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gate1989 descriptive digital-logic boolean-algebra

4.4.5 Boolean Algebra: GATE1992-02-i

https://gateoverflow.in/555

Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:
The operation which is commutative but not associative is:

A. AND B. OR C. EX-OR D. NAND

gate1992 easy digital-logic boolean-algebra

4.4.6 Boolean Algebra: GATE1994-4

https://gateoverflow.in/2500

A. Let $*$ be a Boolean operation defined as $A * B = AB + \overline{A}\,\overline{B}$. If $C = A * B$ then evaluate and fill in the blanks:
   i. $A * A =$____
   ii. $C * A =$____
B. Solve the following boolean equations for the values of A, B and C:
   $AB + \overline{A}C = 1$
   $AC + B = 0$

gate1994 digital-logic normal boolean-algebra

4.4.7 Boolean Algebra: GATE1995-2.5

https://gateoverflow.in/2617

What values of A, B, C and D satisfy the following simultaneous Boolean equations?
$\overline{A} + AB = 0, AB = AC, AB + A\overline{C} + CD = \overline{C}D$

A. $A = 1, B = 0, C = 0, D = 1$ B. $A = 1, B = 1, C = 0, D = 0$
C. $A = 1, B = 0, C = 1, D = 1$ D. $A = 1, B = 0, C = 0, D = 0$

gate1995 digital-logic boolean-algebra easy

4.4.8 Boolean Algebra: GATE1997-2-1

https://gateoverflow.in/2227

Let $*$ be defined as $x * y = \bar{x} + y$. Let $z = x * y$. Value of $z * x$ is

A. $\bar{x} + y$ B. x C. 0 D. 1

gate1997 digital-logic normal boolean-algebra

4.4.9 Boolean Algebra: GATE1998-1.13

https://gateoverflow.in/1650

What happens when a bit-string is XORed with itself n-times as shown:
$[B \oplus (B \oplus (B \oplus (B \ldots n \text{ times}]$

A. complements when n is even B. complements when n is odd
C. divides by 2^n always D. remains unchanged when n is even

gate1998 digital-logic normal boolean-algebra

4.4.10 Boolean Algebra: GATE1998-2.8

https://gateoverflow.in/1680

Which of the following operations is commutative but not associative?

A. AND B. OR C. NAND D. EXOR

gate1998 digital-logic easy boolean-algebra

4.4.11 Boolean Algebra: GATE1999-1.7

https://gateoverflow.in/1460

Which of the following expressions is not equivalent to $\bar{x}$?

A. x NAND x B. x NOR x C. x NAND 1 D. x NOR 1

gate1999 digital-logic easy boolean-algebra

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4.4.12 Boolean Algebra: GATE2000-2.10

https://gateoverflow.in/657

The simultaneous equations on the Boolean variables x, y, z and w,

- $x + y + z = 1$
- $xy = 0$
- $xz + w = 1$
- $xy + \bar{z}\bar{w} = 0$

have the following solution for x, y, z and w, respectively:

A. 0 1 0 0
B. 1 1 0 1
C. 1 0 1 1
D. 1 0 0 0

gate2000 digital-logic boolean-algebra easy

4.4.13 Boolean Algebra: GATE2002-2-3

https://gateoverflow.in/833

Let $f(A, B) = A' + B$. Simplified expression for function $f(f(x + y, y), z)$ is

A. $x' + z$
B. xyz
C. $xy' + z$
D. None of the above

gate2002 digital-logic boolean-algebra normal

4.4.14 Boolean Algebra: GATE2004-17

https://gateoverflow.in/1014

A Boolean function $x'y' + xy + x'y$ is equivalent to

A. $x' + y'$
B. $x + y$
C. $x + y'$
D. $x' + y$

gate2004 digital-logic easy boolean-algebra

4.4.15 Boolean Algebra: GATE2004-IT-44

https://gateoverflow.in/3687

The function $A\bar{B}C + \bar{A}BC + AB\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C}$ is equivalent to

A. $A\bar{C} + AB + \bar{A}C$
B. $A\bar{B} + A\bar{C} + \bar{A}C$
C. $\bar{A}B + A\bar{C} + A\bar{B}$
D. $\bar{A}B + AC + A\bar{B}$

gate2004-it digital-logic boolean-algebra easy

4.4.16 Boolean Algebra: GATE2005-IT-7

https://gateoverflow.in/3752

Which of the following expressions is equivalent to $(A \oplus B) \oplus C$

A. $(A + B + C)(\bar{A} + \bar{B} + \bar{C})$
B. $(A + B + C)(\bar{A} + \bar{B} + C)$
C. $ABC + \bar{A}(B \oplus C) + \bar{B}(A \oplus C)$
D. None of these

gate2005-it digital-logic normal boolean-algebra

4.4.17 Boolean Algebra: GATE2007-32

https://gateoverflow.in/1230

Let $f(w, x, y, z) = \sum(0, 4, 5, 7, 8, 9, 13, 15)$. Which of the following expressions are NOT equivalent to f?

P: $x'y'z' + w'xy' + wy'z + xz$

Q: $w'y'z' + wx'y' + xz$

R: $w'y'z' + wx'y' + xyz + xy'z$

S: $x'y'z' + wx'y' + w'y$

A. P only
B. Q and S
C. R and S
D. S only

gate2007 digital-logic normal boolean-algebra

4.4.18 Boolean Algebra: GATE2007-33

https://gateoverflow.in/1231

Define the connective $*$ for the Boolean variables X and Y as:

$$X * Y = XY + X'Y'.$$

Let $Z = X * Y$. Consider the following expressions P, Q and R.

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$$P : X = Y * Z, Q : Y = X * Z, R : X * Y * Z = 1$$

Which of the following is **TRUE**?

A. Only P and Q are valid.
B. Only Q and R are valid.
C. Only P and R are valid.
D. All P, Q, R are valid.

gate2007 digital-logic normal boolean-algebra

4.4.19 Boolean Algebra: GATE2008-26

https://gateoverflow.in/424

If P, Q, R are Boolean variables, then
$(P + \bar{Q})(P.\bar{Q} + P.R)(\bar{P}.\bar{R} + \bar{Q})$ simplifies to

A. $P.\bar{Q}$ B. $P.\bar{R}$ C. $P.\bar{Q} + R$ D. $P.\bar{R} + Q$

gate2008 easy digital-logic boolean-algebra

4.4.20 Boolean Algebra: GATE2012-6

https://gateoverflow.in/38

The truth table

X	Y	(X,Y)
0	0	0
0	1	0
1	0	1
1	1	1

represents the Boolean function

A. X B. $X + Y$ C. $X \oplus Y$ D. Y

gate2012 digital-logic easy boolean-algebra

4.4.21 Boolean Algebra: GATE2013-21

https://gateoverflow.in/1532

Which one of the following expressions does **NOT** represent exclusive NOR of x and y?

A. $xy + x'y'$
B. $x \oplus y'$
C. $x' \oplus y$
D. $x' \oplus y'$

gate2013 digital-logic easy boolean-algebra

4.4.22 Boolean Algebra: GATE2014-3-55

https://gateoverflow.in/2090

Let $\oplus$ denote the exclusive OR (XOR) operation. Let '1' and '0' denote the binary constants. Consider the following Boolean expression for F over two variables P and Q:

$$F(P, Q) = ((1 \oplus P) \oplus (P \oplus Q)) \oplus ((P \oplus Q) \oplus (Q \oplus 0))$$

The equivalent expression for F is

A. $P + Q$ B. $\overline{P + Q}$ C. $P \oplus Q$ D. $\overline{P \oplus Q}$

gate2014-3 digital-logic normal boolean-algebra

4.4.23 Boolean Algebra: GATE2015-2-37

https://gateoverflow.in/8162

The number of min-terms after minimizing the following Boolean expression is _____.

[D'+AB'+A'C+AC'D+A'C'D]'

gate2015-2 digital-logic boolean-algebra normal numerical-answers

4.4.24 Boolean Algebra: GATE2016-1-06

https://gateoverflow.in/39629

Consider the Boolean operator # with the following properties :
x#0=x, x#1=$\overline{x}$,x#x=0 and x# $\overline{x}$=1. Then x#y is equivalent to

A. $x\overline{y} + \overline{x}y$
B. $x\overline{y} + \overline{x}\,\overline{y}$
C. $\overline{x}y + xy$
D. $xy + \overline{x}\,\overline{y}$

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gate2016-1 digital-logic boolean-algebra easy

4.4.25 Boolean Algebra: GATE2016-2-08

https://gateoverflow.in/39540

Let, $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$ where x_1, x_2, x_3, x_4 are Boolean variables, and $\oplus$ is the XOR operator.
Which one of the following must always be **TRUE**?

A. $x_1x_2x_3x_4 = 0$
B. $x_1x_3 + x_2 = 0$
C. $\bar{x}_1 \oplus \bar{x}_3 = \bar{x}_2 \oplus \bar{x}_4$
D. $x_1 + x_2 + x_3 + x_4 = 0$

gate2016-2 digital-logic boolean-algebra normal

4.4.26 Boolean Algebra: GATE2017-2-27

https://gateoverflow.in/118494

If w, x, y, z are Boolean variables, then which one of the following is INCORRECT?

A. $wx + w(x + y) + x(x + y) = x + wy$
B. $\overline{w\bar{x}(y + \bar{z})} + \bar{w}x = \bar{w} + x + \bar{y}z$
C. $(w\bar{x}(y + x\bar{z}) + \bar{w}\bar{x})y = x\bar{y}$
D. $(w + y)(wxy + wyz) = wxy + wyz$

gate2017-2 digital-logic boolean-algebra normal

4.4.27 Boolean Algebra: GATE2018-4

https://gateoverflow.in/204078

Let $\oplus$ and $\odot$ denote the Exclusive OR and Exclusive NOR operations, respectively. Which one of the following is NOT CORRECT?

A. $\overline{P \oplus Q} = P \odot Q$
B. $\overline{P} \oplus Q = P \odot Q$
C. $\overline{P} \oplus \overline{Q} = P \oplus Q$
D. $P \oplus \overline{P} \oplus Q = (P \odot \overline{P} \odot \overline{Q})$

gate2018 digital-logic normal boolean-algebra

4.4.28 Boolean Algebra: GATE2019-6

https://gateoverflow.in/302842

Which one of the following is NOT a valid identity?

A. $(x \oplus y) \oplus z = x \oplus (y \oplus z)$
B. $(x + y) \oplus z = x \oplus (y + z)$
C. $x \oplus y = x + y$, if $xy = 0$
D. $x \oplus y = (xy + x'y')'$

gate2019 digital-logic boolean-algebra

4.4.29 Boolean Algebra: TIFR2010-B-21

https://gateoverflow.in/18621

For $x \in \{0,1\}$, let $\neg x$ denote the negation of x, that is

$$\neg\, x = \begin{cases} 1 & \text{iff } x = 0 \\ 0 & \text{iff } x = 1 \end{cases}$$

.

If $x \in \{0,1\}^n$, then $\neg\, x$ denotes the component wise negation of x; that is:

$$(\neg\, x)_i = (\neg\, x_i \mid i \in [1..n])$$

Consider a circuit C, computing a function $f : \{0,1\}^n \to \{0,1\}$ using **AND** ($\wedge$), **OR** ($\vee$),and **NOT** ($\neg$) gates. Let D be the circuit obtained from C by replacing each **AND** gate by an **OR** gate and replacing each **OR** gate by an **AND**. Suppose D computes the function g. Which of the following is true for all inputs x?

A. $g(x) = \neg\, f(x)$
B. $g(x) = f(x) \wedge f(\neg x)$
C. $g(x) = f(x) \vee f(\neg x)$
D. $g(x) = \neg f(\neg x)$
E. None of the above.

tifr2010 digital-logic boolean-algebra

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4.4.30 Boolean Algebra: TIFR2014-B-17

https://gateoverflow.in/27344

Let $f : \{0,1\}^n \to \{0,1\}$ be a boolean function computed by a logical circuit comprising just binary AND and binary OR gates (assume that the circuit does not have any feedback). Let PARITY : $\{0,1\}^n \to \{0,1\}$ be the boolean function that outputs 1 if the total number of input bits set to 1 is odd. Similarly, let MAJORITY be the boolean function that outputs 1 if the number of input bits that are set to 1 is at least as large as the number of input bits that are set to 0. Then, which of the following is NOT possible?

a. $f(0,0,\ldots,0) = f(1,1,\ldots,1) = 0$.
b. $f(0,0,\ldots,0) = f(1,1.\ldots,1) = 1$
c. f is the MAJORITY function.
d. f is the PARITY function.
e. f outputs 1 at exactly one assignment of the input bits.

tifr2014 boolean-algebra

4.4.31 Boolean Algebra: TIFR2016-B-1

https://gateoverflow.in/97626

A Boolean formula is said to be a $tautology$ if it evaluates to TRUE for all assignments to its variables. Which one of the following is NOT a tautology?

A. $((p \vee q) \wedge (r \vee s)) \Rightarrow ((p \wedge r) \vee q \vee s)$
B. $((p \vee q) \wedge (r \vee s)) \Rightarrow (q \vee s)$
C. $((p \vee q) \wedge (r \vee s)) \Rightarrow (r \vee q \vee s)$
D. $((p \vee q) \wedge (r \vee s)) \Rightarrow (p \vee q \vee s)$
E. $((p \vee q) \wedge (r \vee s)) \Rightarrow (p \vee q)$

tifr2016 boolean-algebra

4.5 Booths Algorithm (6)

4.5.1 Booths Algorithm: GATE1990-8b

https://gateoverflow.in/85671

State the Booth's algorithm for multiplication of two numbers. Draw a block diagram for the implementation of the Booth's algorithm for determining the product of two 8-bit signed numbers.

gate1990 descriptive digital-logic booths-algorithm

4.5.2 Booths Algorithm: GATE1996-1.23

https://gateoverflow.in/2727

Booth’s algorithm for integer multiplication gives worst performance when the multiplier pattern is

A. 101010 ….. 1010
B. 100000 ….. 0001
C. 111111 ….. 1111
D. 011111 ….. 1110

gate1996 digital-logic booths-algorithm normal

4.5.3 Booths Algorithm: GATE1999-1.20

https://gateoverflow.in/1473

Booth's coding in 8 bits for the decimal number -57 is:

A. $0-100+1000$ B. $0-100+100-1$ C. $0-1+100-10+1$ D. $00-10+100-1$

gate1999 digital-logic number-representation booths-algorithm normal

add last bit =0, then P= In 2's compliment form, it is: 11000111 = -57
after adding 0, its P= 110001110, its booth's value= 0-100+100-1

4.5.4 Booths Algorithm: GATE2005-IT-8

https://gateoverflow.in/3753

Using Booth's Algorithm for multiplication, the multiplier -57 will be recoded as

A. 0 -1 00 1 0 0 -1
B. 1 1 0 0 0 1 1 1
C. 0 -1 0 0 10 0 0
D. 0 1 0 0 -1 0 0 1

gate2005-it digital-logic booths-algorithm normal

4.5.5 Booths Algorithm: GATE2006-IT-38

https://gateoverflow.in/3577

When multiplicand Y is multiplied by multiplier $X = x_{n-1}x_{n-2}\ldots x_0$ using bit-pair recoding in Booth's algorithm, partial products are generated according to the following table.

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Row	x_{i+1}	x_i	x_{i-1}	Partial Product
1	0	0	0	0
2	0	0	1	Y
3	0	1	0	Y
4	0	1	1	2Y
5	1	0	0	?
6	1	0	1	-Y
7	1	1	0	-Y
8	1	1	1	?

The partial products for rows 5 and 8 are

A. $2Y$ and Y B. $-2Y$ and $2Y$ C. $-2Y$ and 0 D. 0 and Y

gate2006-it digital-logic booths-algorithm difficult

4.5.6 Booths Algorithm: GATE2008-IT-42

https://gateoverflow.in/3352

The two numbers given below are multiplied using the Booth's algorithm.

Multiplicand : 0101 1010 1110 1110
Multiplier: 0111 0111 1011 1101

How many additions/Subtractions are required for the multiplication of the above two numbers?

A. 6 B. 8 C. 10 D. 12

gate2008-it digital-logic booths-algorithm normal

4.6 Canonical Normal Form (8)

4.6.1 Canonical Normal Form: GATE1990-5-a

https://gateoverflow.in/85396

Find the minimum product of sums of the following expression

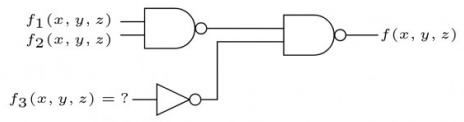
$$f = ABC + \bar{A}\bar{B}\bar{C}$$

gate1990 digital-logic canonical-normal-form descriptive

4.6.2 Canonical Normal Form: GATE2002-2-1

https://gateoverflow.in/831

Consider the following logic circuit whose inputs are functions f_1, f_2, f_3 and output is f



Given that

- $f_1(x, y, z) = \Sigma(0, 1, 3, 5)$
- $f_2(x, y, z) = \Sigma(6, 7)$, and
- $f(x, y, z) = \Sigma(1, 4, 5)$.

f_3 is

A. $\Sigma(1, 4, 5)$ B. $\Sigma(6, 7)$
C. $\Sigma(0, 1, 3, 5)$ D. None of the above

gate2002 digital-logic normal canonical-normal-form circuit-output

4.6.3 Canonical Normal Form: GATE2008-8

https://gateoverflow.in/406

Given f_1, f_3 and f in canonical sum of products form (in decimal) for the circuit

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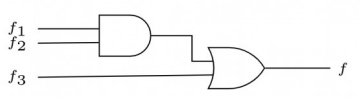

$f_1 = \Sigma m(4,5,6,7,8)$
$f_3 = \Sigma m(1,6,15)$
$f = \Sigma m(1,6,8,15)$
then f_2 is

A. $\Sigma m(4,6)$
B. $\Sigma m(4,8)$
C. $\Sigma m(6,8)$
D. $\Sigma m(4,6,8)$

gate2008 digital-logic canonical-normal-form easy

4.6.4 Canonical Normal Form: GATE2010-6

https://gateoverflow.in/2177

The minterm expansion of $f(P,Q,R) = PQ + Q\bar{R} + P\bar{R}$ is

A. $m_2 + m_4 + m_6 + m_7$
B. $m_0 + m_1 + m_3 + m_5$
C. $m_0 + m_1 + m_6 + m_7$
D. $m_2 + m_3 + m_4 + m_5$

gate2010 digital-logic canonical-normal-form normal

4.6.5 Canonical Normal Form: GATE2015-3-43

https://gateoverflow.in/8503

The total number of prime implicants of the function $f(w,x,y,z) = \sum(0,2,4,5,6,10)$ is _____

gate2015-3 digital-logic canonical-normal-form normal numerical-answers

4.6.6 Canonical Normal Form: GATE2015-3-44

https://gateoverflow.in/8504

Given the function $F = P' + QR$, where F is a function in three Boolean variables P, Q and R and $P' = !P$, consider the following statements.

$(S1) F = \sum(4,5,6)$
$(S2) F = \sum(0,1,2,3,7)$
$(S3) F = \Pi(4,5,6)$
$(S4) F = \Pi(0,1,2,3,7)$

Which of the following is true?

A. (S1)-False, (S2)-True, (S3)-True, (S4)-False
B. (S1)-True, (S2)-False, (S3)-False, (S4)-True
C. (S1)-False, (S2)-False, (S3)-True, (S4)-True
D. (S1)-True, (S2)-True, (S3)-False, (S4)-False

gate2015-3 digital-logic canonical-normal-form normal

4.6.7 Canonical Normal Form: GATE2019-50

https://gateoverflow.in/302798

What is the minimum number of 2-input NOR gates required to implement a 4 -variable function expressed in sum-of-minterms form as $f = \Sigma(0,2,5,7,8,10,13,15)$? Assume that all the inputs and their complements are available. Answer: _____

gate2019 numerical-answers digital-logic canonical-normal-form

4.6.8 Canonical Normal Form: TIFR2015-B-9

https://gateoverflow.in/30030

A Boolean expression is an expression made out of propositional letters (such as p, q, r) and operators $\wedge$, $\vee$ and $\neg$; e.g. $p \wedge \neg(q \vee \neg r)$. An expression is said to be in sum of product form (also called disjunctive normal form) if all $\neg$ occur just before letters and no $\vee$ occurs in scope of $\wedge$; e.g. $(p \wedge \neg q) \vee (\neg p \wedge q)$. The expression is said to be in product of sum form (also called conjunctive normal form) if all negations occur just before letters and no $\wedge$ occurs in the scope of $\vee$; e.g. $(p \vee \neg q) \wedge (\neg p \vee q)$. Which of the following is not correct?

A. Every Boolean expression is equivalent to an expression in sum of product form.
B. Every Boolean expression is equivalent to an expression in product of sum form.

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C. Every Boolean expression is equivalent to an expression without $\vee$ operator.
D. Every Boolean expression is equivalent to an expression without $\wedge$ operator.
E. Every Boolean expression is equivalent to an expression without $\neg$ operator.

tifr2015 canonical-normal-form

4.7 Carry Generator (2)

4.7.1 Carry Generator: GATE2006-36

https://gateoverflow.in/1294

Given two three bit numbers $a_2a_1a_0$ and $b_2b_1b_0$ and c the carry in, the function that represents the c*arry* generate function when these two numbers are added is:

A. $a_2b_2 + a_2a_1b_1 + a_2a_1a_0b_0 + a_2a_0b_1b_0 + a_1b_2b_1 + a_1a_0b_2b_0 + a_0b_2b_1b_0$
B. $a_2b_2 + a_2b_1b_0 + a_2a_1b_1b_0 + a_1a_0b_2b_1 + a_1a_0b_2 + a_1a_0b_2b_0 + a_2a_0b_1b_0$
C. $a_2 + b_2 + (a_2 \oplus b_2)(a_1 + b_1 + (a_1 \oplus b_1) + (a_0 + b_0))$
D. $a_2b_2 + \overline{a_2}a_1b_1 + \overline{a_2a_1}a_0b_0 + \overline{a_2}a_0\overline{b_1}b_0 + a_1\overline{b_2}b_1 + \overline{a_1}a_0\overline{b_2}b_0 + a_0\overline{b_2b_1}b_0$

gate2006 digital-logic normal carry-generator

4.7.2 Carry Generator: GATE2007-35

https://gateoverflow.in/1233

In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs A_i and B_i are given by:

$$P_i = A_i \oplus B_i \text{ and } G_i = A_iB_i$$

The expressions for the sum bit S_i and the carry bit C_{i+1} of the look ahead carry adder are given by:

$$S_i = P_i \oplus C_i \text{ and } C_{i+1} = G_i + P_iC_i, \text{ where } C_0 \text{ is the input carry.}$$

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S_3, S_2, S_1, S_0 and C_4 as its outputs are respectively:

A. $6, 3$ B. $10, 4$ C. $6, 4$ D. $10, 5$

gate2007 digital-logic normal carry-generator adder

4.8 Circuit Output (38)

4.8.1 Circuit Output: GATE1989-4-ix

https://gateoverflow.in/88164

Provide short answers to the following questions:

Explain the behaviour of the following logic circuit (Fig.4) with level input A and output B

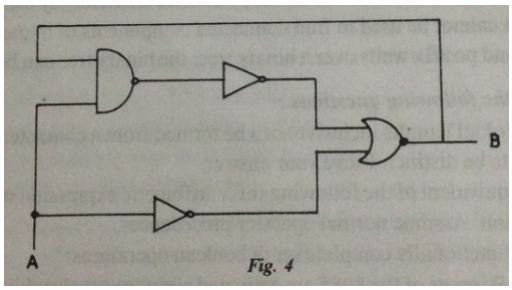

Fig. 4

gate1989 descriptive digital-logic circuit-output

4.8.2 Circuit Output: GATE1990-3-i

https://gateoverflow.in/84051

Choose the correct alternatives (More than one may be correct).

Two NAND gates having open collector outputs are tied together as shown in below figure.

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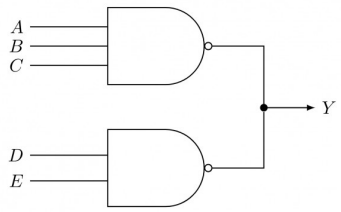


The logic function Y, implemented by the circuit is,

A. $Y = ABC + DE$
B. $Y = \overline{ABC + DE}$
C. $Y = ABC.DE$
D. $Y = \overline{ABC.DE}$

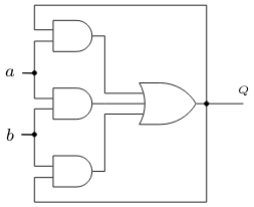
gate1990 normal digital-logic circuit-output

4.8.3 Circuit Output: GATE1991-5-a

https://gateoverflow.in/531

Analyse the circuit in Fig below and complete the following table

a	b	Q_n
0	0	
0	1	
1	0	
1	1	

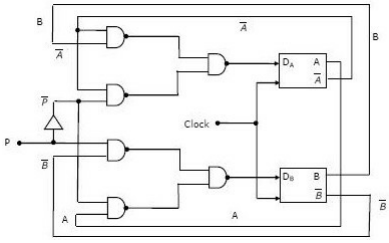


gate1991 digital-logic normal circuit-output

4.8.4 Circuit Output: GATE1993-19

https://gateoverflow.in/2316

A control algorithm is implemented by the NAND – gate circuitry given in figure below, where A and B are state variable implemented by D flip-flops, and P is control input. Develop the state transition table for this controller.



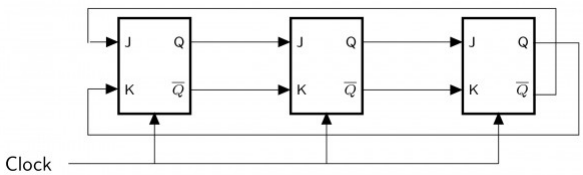
gate1993 digital-logic circuit-output normal descriptive

4.8.5 Circuit Output: GATE1993-6-3

https://gateoverflow.in/17237

Multiple choices can be correct. Mark all of them.

For the initial state of 000, the function performed by the arrangement of the $J-K$ flip-flops in figure is:



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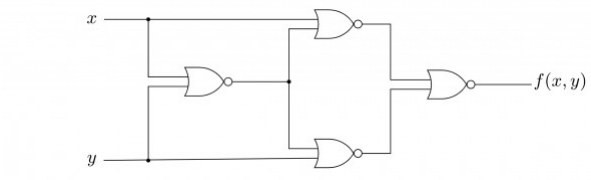
A. Shift Register
B. $Mod-3$ Counter
C. $Mod-6$ Counter
D. $Mod-2$ Counter
E. None of the above

gate1993 digital-logic circuit-output normal

4.8.6 Circuit Output: GATE1993-6.1

https://gateoverflow.in/2288

Identify the logic function performed by the circuit shown in figure.



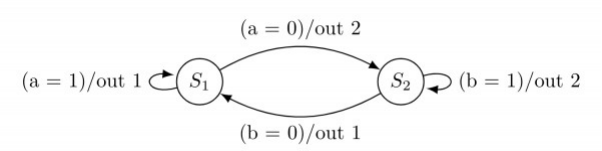
A. exclusive OR B. exclusive NOR C. NAND D. NOR E. None of the above

gate1993 digital-logic circuit-output normal

4.8.7 Circuit Output: GATE1993-6.2

https://gateoverflow.in/17235

If the state machine described in figure should have a stable state, the restriction on the inputs is given by



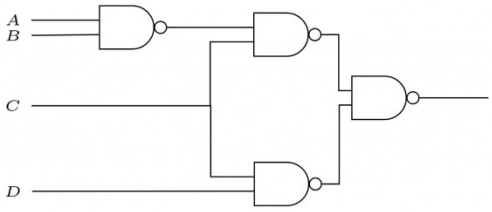
A. $a.b=1$
B. $a+b=1$
C. $\bar{a}+\bar{b}=0$
D. $\overline{a.b}=1$
E. $\overline{a+b}=1$

gate1993 digital-logic normal circuit-output

4.8.8 Circuit Output: GATE1994-1.8

https://gateoverflow.in/2445

The logic expression for the output of the circuit shown in figure below is:



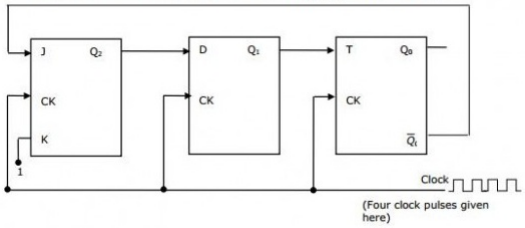
A. $\overline{AC}+\overline{BC}+CD$
B. $A\overline{C}+B\overline{C}+CD$
C. $ABC+\overline{C}\ \overline{D}$
D. $\overline{A}\ \overline{B}+\overline{B}\ \overline{C}+CD$

gate1994 digital-logic circuit-output normal

4.8.9 Circuit Output: GATE1994-11

https://gateoverflow.in/2507

Find the contents of the flip-flop Q_2, Q_1 and Q_0 in the circuit of figure, after giving four clock pulses to the clock terminal. Assume $Q_2Q_1Q_0=000$ initially.



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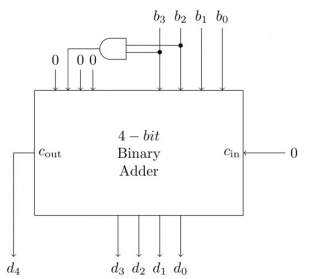
gate1994 digital-logic circuit-output normal

4.8.10 Circuit Output: GATE1996-2.21

https://gateoverflow.in/2750

Consider the circuit in below figure which has a four bit binary number $b_3b_2b_1b_0$ as input and a five bit binary number, $d_4d_3d_2d_1d_0$ as output.



A. Binary to Hex conversion

B. Binary to BCD conversion

C. Binary to Gray code conversion

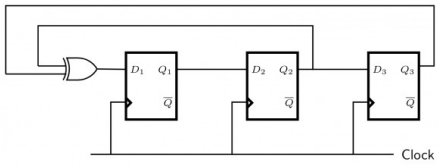
D. Binary to $radix-12$ conversion

gate1996 digital-logic circuit-output normal

4.8.11 Circuit Output: GATE1996-24-a

https://gateoverflow.in/2776

Consider the synchronous sequential circuit in the below figure



Draw a state diagram, which is implemented by the circuit. Use the following names for the states corresponding to the values of flip-flops as given below.

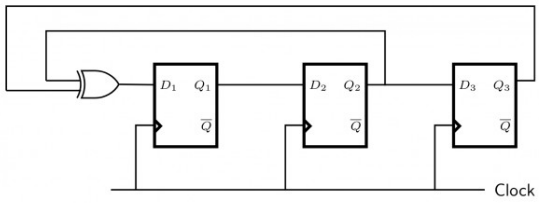
Q1	Q2	Q3	State
0	0	0	S_0
0	0	1	S_1
–	–	–	–
–	–	–	–
–	–	–	–
1	1	1	S_7

gate1996 digital-logic circuit-output normal

4.8.12 Circuit Output: GATE1996-24-b

https://gateoverflow.in/203691

Consider the synchronous sequential circuit in the below figure



Given that the initial state of the circuit is S_4, identify the set of states, which are not reachable.

gate1996 normal digital-logic circuit-output

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4.8.13 Circuit Output: GATE1997-5.5

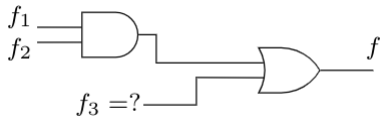
https://gateoverflow.in/2256

Consider a logic circuit shown in figure below. The functions f_1, f_2 and f (in canonical sum of products form in decimal notation) are :

$f_1(w,x,y,z) = \sum 8,9,10$

$f_2(w,x,y,z) = \sum 7,8,12,13,14,15$

$f(w,x,y,z) = \sum 8,9$



The function f_3 is

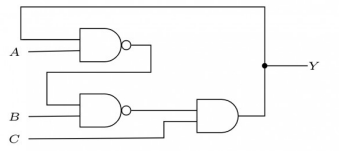
A. $\sum 9,10$ B. $\sum 9$ C. $\sum 1,8,9$ D. $\sum 8,10,15$

gate1997 digital-logic circuit-output normal

4.8.14 Circuit Output: GATE1999-2.8

https://gateoverflow.in/1486

Consider the circuit shown below. In a certain steady state, the line Y is at $'1'$. What are the possible values of A, B and C in this state?



A. $A=0, B=0, C=1$ B. $A=0, B=1, C=1$

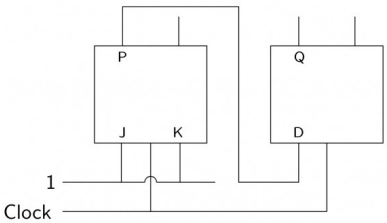
C. $A=1, B=0, C=1$ D. $A=1, B=1, C=1$

gate1999 digital-logic circuit-output normal

4.8.15 Circuit Output: GATE2000-2.12

https://gateoverflow.in/659

The following arrangement of master-slave flip flops



has the initial state of P, Q as $0, 1$ (respectively). After three clock cycles the output state P, Q is (respectively),

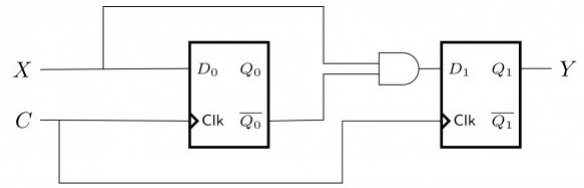
A. $1,0$ B. $1,1$ C. $0,0$ D. $0,1$

gate2000 digital-logic circuit-output normal flip-flop

4.8.16 Circuit Output: GATE2001-2.8

https://gateoverflow.in/726

Consider the following circuit with initial state $Q_0 = Q_1 = 0$. The D Flip-flops are positive edged triggered and have set up times 20 nanosecond and hold times 0.



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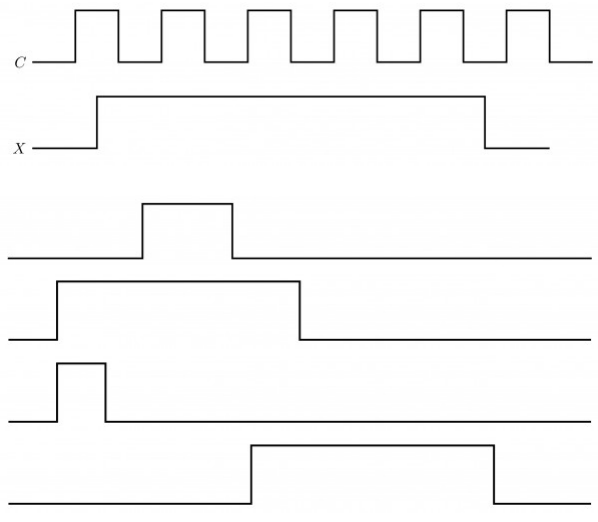
Consider the following timing diagrams of X and C. The clock period of $C \geq 40$ nanosecond. Which one is the correct plot of Y?

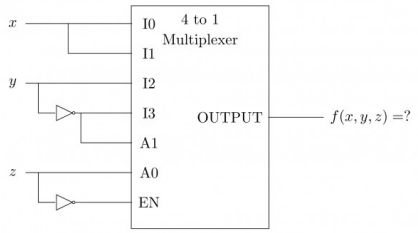


gate2001 digital-logic circuit-output normal

4.8.17 Circuit Output: GATE2002-2.2

https://gateoverflow.in/832

Consider the following multiplexer where $I0, I1, I2, I3$ are four data input lines selected by two address line combinations $A1A0 = 00, 01, 10, 11$ respectively and f is the output of the multiplexor. EN is the Enable input.



The function $f(x, y, z)$ implemented by the above circuit is

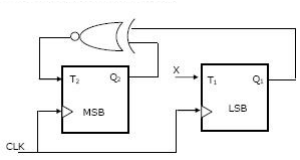
A. xyz' B. $xy + z$ C. $x + y$ D. None of the above

gate2002 digital-logic circuit-output normal

4.8.18 Circuit Output: GATE2004-61

https://gateoverflow.in/1056

Consider the partial implementation of a 2-bit counter using T flip-flops following the sequence 0-2-3-1-0, as shown below.



To complete the circuit, the input X should be

A. Q_2^c B. $Q_2 + Q_1$ C. $(Q_1 + Q_2)^c$ D. $Q_1 \oplus Q_2$

gate2004 digital-logic circuit-output normal

4.8.19 Circuit Output: GATE2005-15

https://gateoverflow.in/1351

Consider the following circuit.

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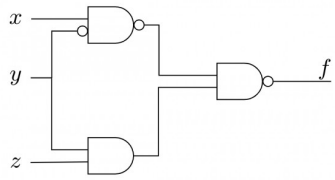


Which one of the following is TRUE?

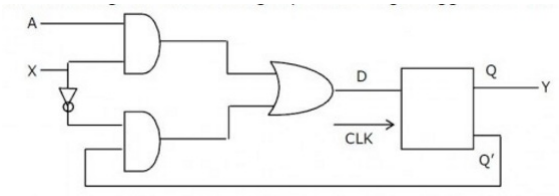
A. f is independent of x
B. f is independent of y
C. f is independent of z
D. None of x, y, z is redundant

gate2005 digital-logic circuit-output normal

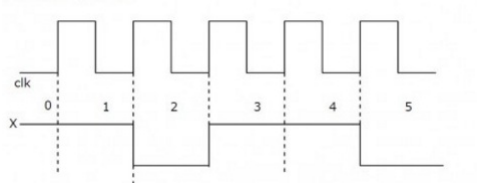
4.8.20 Circuit Output: GATE2005-62

https://gateoverflow.in/264

Consider the following circuit involving a positive edge triggered D FF.



Consider the following timing diagram. Let A_i represents the logic level on the line a in the i-th clock period.



Let A' represent the compliment of A. The correct output sequence on Y over the clock periods 1 through 5 is:

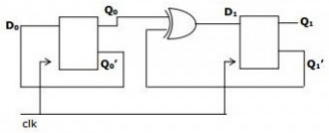
A. $A_0A_1A_1'A_3A_4$
B. $A_0A_1A_2'A_3A_4$
C. $A_1A_2A_2'A_3A_4$
D. $A_1A_2'A_3A_4A_5'$

gate2005 digital-logic circuit-output normal

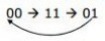
4.8.21 Circuit Output: GATE2005-64

https://gateoverflow.in/1387

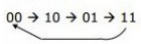
Consider the following circuit:

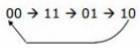


The flip-flops are positive edge triggered D FFs. Each state is designated as a two-bit string Q_0Q_1. Let the initial state be 00. The state transition sequence is

A. 

B. 

C. 

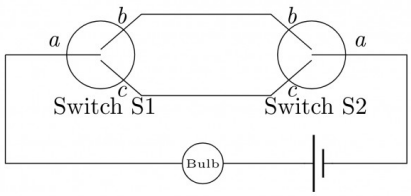
D. 

gate2005 digital-logic circuit-output

4.8.22 Circuit Output: GATE2005-IT-10

https://gateoverflow.in/3755

A two-way switch has three terminals a, b and c. In ON position (logic value 1), a is connected to b, and in OFF position, a is connected to c. Two of these two-way switches $S1$ and $S2$ are connected to a bulb as shown below.



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Which of the following expressions, if true, will always result in the lighting of the bulb ?

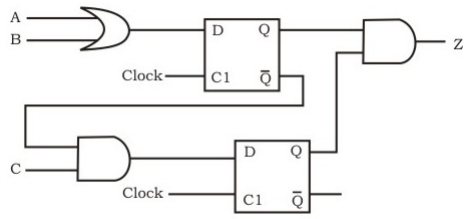
A. $S1.\overline{\overline{S2}}$
B. $S1 + S2$
C. $\overline{\overline{S1 \oplus S2}}$
D. $S1 \oplus S2$

gate2005-it digital-logic circuit-output normal

4.8.23 Circuit Output: GATE2005-IT-43

https://gateoverflow.in/3804

Which of the following input sequences will always generate a 1 at the output z at the end of the third cycle?



A.

A	B	C
0	0	0
1	0	1
1	1	1

B.

A	B	C
1	0	1
1	1	0
1	1	1

C.

A	B	C
0	1	1
1	0	1
1	1	1

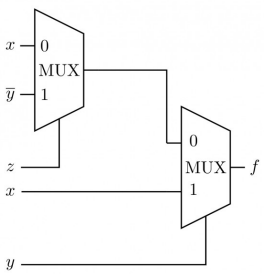
D.

A	B	C
0	0	1
1	1	0
1	1	1

gate2005-it digital-logic circuit-output normal

4.8.24 Circuit Output: GATE2006-35

https://gateoverflow.in/1292



Consider the circuit above. Which one of the following options correctly represents $f(x, y, z)$

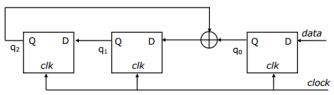
A. $x\bar{z} + xy + \bar{y}z$
B. $x\bar{z} + xy + \overline{yz}$
C. $xz + xy + \overline{yz}$
D. $xz + x\bar{y} + \bar{y}z$

gate2006 digital-logic circuit-output normal

4.8.25 Circuit Output: GATE2006-37

https://gateoverflow.in/1295

Consider the circuit in the diagram. The $\oplus$ operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).



The following data: 100110000 is supplied to the "data" terminal in nine clock cycles. After that the values of $q_2 q_1 q_0$ are:

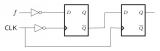
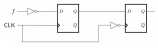
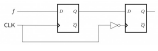
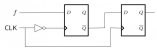
A. 000
B. 001
C. 010
D. 101

gate2006 digital-logic circuit-output easy

4.8.26 Circuit Output: GATE2006-8

https://gateoverflow.in/887

You are given a free running clock with a duty cycle of 50% and a digital waveform f which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip-flops) will delay the phase of f by 180°?

A. 
B. 
C. 
D. 

gate2006 digital-logic normal circuit-output

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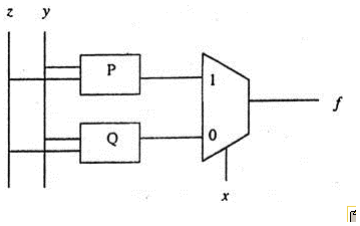
4.8.27 Circuit Output: GATE2006-IT-36

https://gateoverflow.in/3575

The majority function is a Boolean function $f(x, y, z)$ that takes the value 1 whenever a majority of the variables x, y, z are 1. In the circuit diagram for the majority function shown below, the logic gates for the boxes labeled P and Q are, respectively,



A. XOR, AND B. XOR, XOR C. OR, OR D. OR, AND

gate2006-it digital-logic circuit-output normal

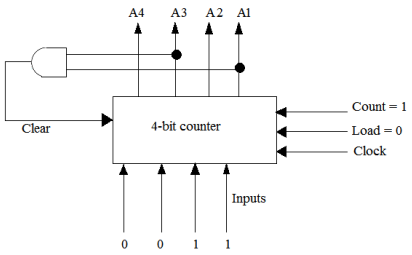
4.8.28 Circuit Output: GATE2007-36

https://gateoverflow.in/1234

The control signal functions of a $4\text{-}bit$ binary counter are given below (where X is "don't care"):

Clear	Clock	Load	Count	Function
1	X	X	X	Clear to 0
0	X	0	0	No Change
0	↑	1	X	Load Input
0	↑	0	1	Count Next

The counter is connected as follows:



Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence:

A. $0, 3, 4$ B. $0, 3, 4, 5$ C. $0, 1, 2, 3, 4$ D. $0, 1, 2, 3, 4, 5$

gate2007 digital-logic circuit-output normal

4.8.29 Circuit Output: GATE2007-IT-38

https://gateoverflow.in/3471

The following expression was to be realized using 2-input AND and OR gates. However, during the fabrication all 2-input AND gates were mistakenly substituted by 2-input NAND gates. $(a.b).c + (a'.c).d + (b.c).d + a.d$

What is the function finally realized ?

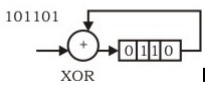
A. 1
B. $a' + b' + c' + d'$
C. $a' + b + c' + d'$
D. $a' + b' + c + d'$

gate2007-it digital-logic circuit-output normal

4.8.30 Circuit Output: GATE2007-IT-40

https://gateoverflow.in/3473

What is the final value stored in the linear feedback shift register if the input is 101101?



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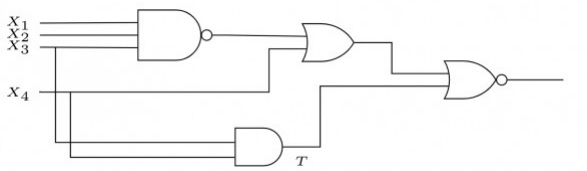
A. 0110 B. 1011 C. 1101 D. 1111

gate2007-it digital-logic circuit-output normal

4.8.31 Circuit Output: GATE2007-IT-45

https://gateoverflow.in/3480

The line T in the following figure is permanently connected to the ground.



Which of the following inputs $(X_1X_2X_3X_4)$ will detect the fault ?

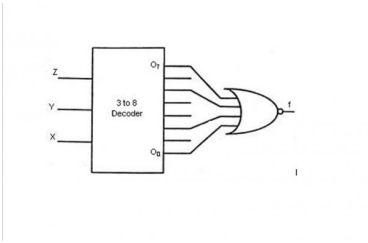
A. 0000 B. 0111 C. 1111 D. None of these

gate2007-it digital-logic circuit-output normal

4.8.32 Circuit Output: GATE2008-IT-9

https://gateoverflow.in/3269

What Boolean function does the circuit below realize?



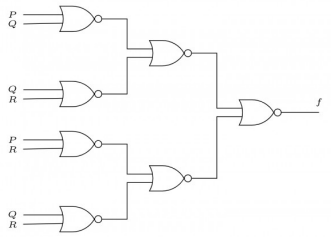
A. $xz + \bar{x}\bar{z}$ B. $x\bar{z} + \bar{x}z$
C. $\bar{x}\bar{y} + yz$ D. $xy + \bar{y}\bar{z}$

gate2008-it digital-logic circuit-output normal

4.8.33 Circuit Output: GATE2010-31

https://gateoverflow.in/2205

What is the boolean expression for the output f of the combinational logic circuit of NOR gates given below?



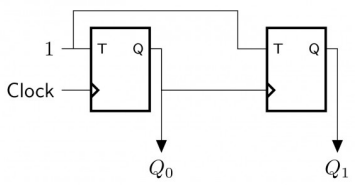
A. $\overline{\overline{Q + R}}$ B. $\overline{\overline{P + Q}}$
C. $\overline{\overline{P + R}}$ D. $\overline{\overline{P + Q + R}}$

gate2010 digital-logic circuit-output normal

4.8.34 Circuit Output: GATE2010-32

https://gateoverflow.in/2206

In the sequential circuit shown below, if the initial value of the output Q_1Q_0 is 00. What are the next four values of Q_1Q_0?



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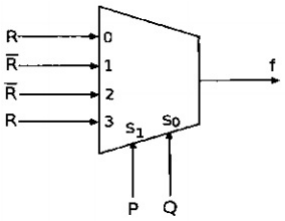
A. 11, 10, 01, 00
B. 10, 11, 01, 00
C. 10, 00, 01, 11
D. 11, 10, 00, 01

gate2010 digital-logic circuit-output normal

4.8.35 Circuit Output: GATE2010-9

https://gateoverflow.in/2182

The Boolean expression of the output f of the multiplexer shown below is



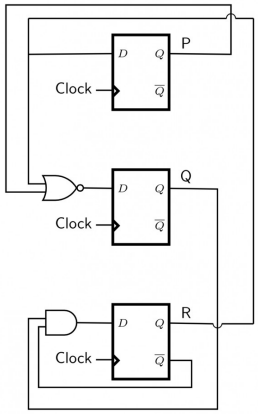
A. $\overline{P \oplus Q \oplus R}$
B. $P \oplus Q \oplus R$
C. $P + Q + R$
D. $\overline{P + Q + R}$

gate2010 digital-logic circuit-output easy

4.8.36 Circuit Output: GATE2011-50

https://gateoverflow.in/2157

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge?

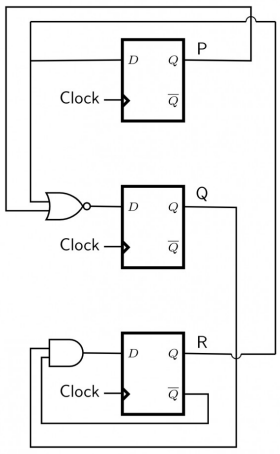
A. 000 B. 001 C. 010 D. 011

gate2011 digital-logic circuit-output flip-flop normal

4.8.37 Circuit Output: GATE2011-51

https://gateoverflow.in/43318

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated

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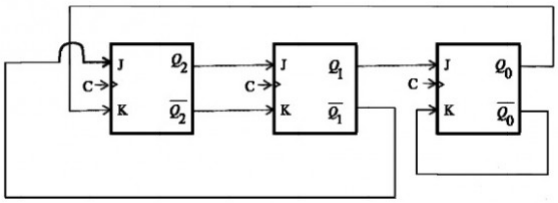
by the counter?

A. 3 B. 4 C. 5 D. 6

gate2011 digital-logic circuit-output normal

4.8.38 Circuit Output: GATE2014-3-45

https://gateoverflow.in/2079



The above synchronous sequential circuit built using JK flip-flops is initialized with $Q_2Q_1Q_0 = 000$. The state sequence for this circuit for the next 3 clock cycles is

A. $001, 010, 011$
B. $111, 110, 101$
C. $100, 110, 111$
D. $100, 011, 001$

gate2014-3 digital-logic circuit-output normal

4.9 Conjunctive Normal Form (1)

4.9.1 Conjunctive Normal Form: GATE2007-48

https://gateoverflow.in/1246

Which of the following is TRUE about formulae in Conjunctive Normal Form?

A. For any formula, there is a truth assignment for which at least half the clauses evaluate to true.
B. For any formula, there is a truth assignment for which all the clauses evaluate to true.
C. There is a formula such that for each truth assignment, at most one-fourth of the clauses evaluate to true.
D. None of the above.

gate2007 digital-logic normal conjunctive-normal-form

4.10 Decoder (1)

4.10.1 Decoder: GATE2007-8, ISRO2011-31

https://gateoverflow.in/1206

How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?

A. 7 B. 8 C. 9 D. 10

gate2007 digital-logic normal isro2011 decoder

4.11 Digital Circuits (8)

4.11.1 Digital Circuits: GATE1992-02-ii

https://gateoverflow.in/556

Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:

All digital circuits can be realized using only

A. Ex-OR gates B. Multiplexers C. Half adders D. OR gates

gate1992 normal digital-logic digital-circuits

4.11.2 Digital Circuits: GATE1996-5

https://gateoverflow.in/2757

A logic network has two data inputs A and B, and two control inputs C_0 and C_1. It implements the function F according to the following table.

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C_1	C_2	**F**
0	0	$\overline{A+B}$
0	1	$A+B$
1	0	$A \oplus B$

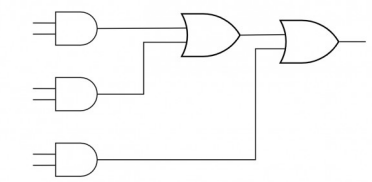
Implement the circuit using one 4 to 1 Multiplexer, one $2-$input Exclusive OR gate, one $2-$input AND gate, one $2-$input OR gate and one Inverter.

gate1996 digital-logic normal digital-circuits

4.11.3 Digital Circuits: GATE2002-7

https://gateoverflow.in/860

A. Express the function $f(x,y,z) = xy' + yz'$ with only one complement operation and one or more AND/OR operations. Draw the logic circuit implementing the expression obtained, using a single NOT gate and one or more AND/OR gates.
B. Transform the following logic circuit (without expressing its switching function) into an equivalent logic circuit that employs only 6 NAND gates each with 2-inputs.

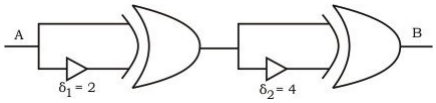


gate2002 digital-logic normal descriptive digital-circuits

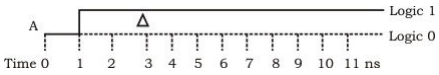
4.11.4 Digital Circuits: GATE2003-47

https://gateoverflow.in/29098

Consider the following circuit composed of XOR gates and non-inverting buffers.



The non-inverting buffers have delays $\delta_1 = 2ns$ and $\delta_2 = 4ns$ as shown in the figure. Both XOR gates and all wires have zero delays. Assume that all gate inputs, outputs, and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns?



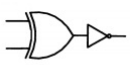
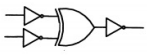
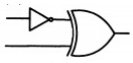
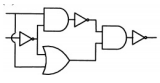
A. 1 B. 2 C. 3 D. 4

gate2003 digital-logic digital-circuits

4.11.5 Digital Circuits: GATE2011-13

https://gateoverflow.in/2115

Which one of the following circuits is **NOT** equivalent to a 2-input $XNOR$ (exclusive NOR) gate?

A. 
B. 
C. 
D. 

gate2011 digital-logic normal digital-circuits

4.11.6 Digital Circuits: GATE2013-5

https://gateoverflow.in/1414

In the following truth table, $V = 1$ if and only if the input is valid.

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Inputs				Outputs		
D_0	D_1	D_2	D_3	X_0	X_1	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

What function does the truth table represent?

A. Priority encoder
B. Decoder
C. Multiplexer
D. Demultiplexer

gate2013 digital-logic normal digital-circuits

4.11.7 Digital Circuits: GATE2014-3-8

https://gateoverflow.in/2042

Consider the following combinational function block involving four Boolean variables x, y, a, b where x, a, b are inputs and y is the output.

```
f(x, a, b, y)
{
    if(x is 1) y = a;
    else y = b;
}
```

Which one of the following digital logic blocks is the most suitable for implementing this function?

A. Full adder
B. Priority encoder
C. Multiplexor
D. Flip-flop

gate2014-3 digital-logic easy digital-circuits

4.11.8 Digital Circuits: TIFR2015-A-4

https://gateoverflow.in/29162

The Boolean function obtained by adding an inverter to each and every input of an AND gate is:

A. OR
B. XOR
C. $NAND$
D. NOR
E. None of the above

tifr2015 digital-logic digital-circuits

4.12 Digital Counter (11)

4.12.1 Digital Counter: GATE1987-10c

https://gateoverflow.in/82452

Give a minimal DFA that performs as a $\mod -3$, 1's counter, i.e. outputs a 1 each time the number of 1's in the input sequence is a multiple of 3.

gate1987 digital-logic digital-counter descriptive

4.12.2 Digital Counter: GATE1994-2-1

https://gateoverflow.in/2468

The number of flip-flops required to construct a binary modulo N counter is _____

gate1994 digital-logic easy digital-counter

4.12.3 Digital Counter: GATE2002-8

https://gateoverflow.in/861

Consider the following circuit. $A = a_2a_1a_0$ and $B = b_2b_1b_0$ are three bit binary numbers input to the circuit. The output is $Z = z_3z_2z_1z_0$. R0, R1 and R2 are registers with loading clock shown. The registers are loaded with their input data with the falling edge of a clock pulse (signal CLOCK shown) and appears as shown. The bits of input number A, B and the full adders are as shown in the circuit. Assume Clock period is greater than the settling time of all circuits.

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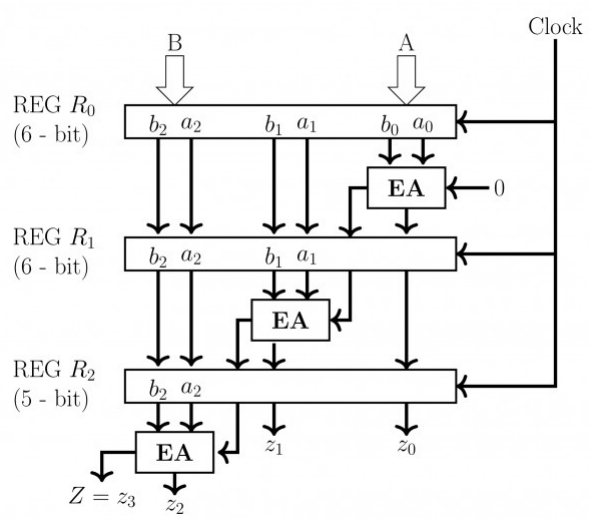


a. For 8 clock pulses on the CLOCK terminal and the inputs A, B as shown, obtain the output Z (sequence of $4 - bit$ values of Z). Assume initial contents of R_0, R_1 and R_2 as all zeros.

A	110	011	111	101	000	000	000	000
B	101	101	011	110	000	000	000	000
Clock No	1	2	3	4	5	6	7	8

b. What does the circuit implement?

gate2002 digital-logic normal descriptive digital-counter

4.12.4 Digital Counter: GATE2005-IT-11

https://gateoverflow.in/3756

How many pulses are needed to change the contents of a 8-bit up counter from 10101100 to 00100111 (rightmost bit is the LSB)?

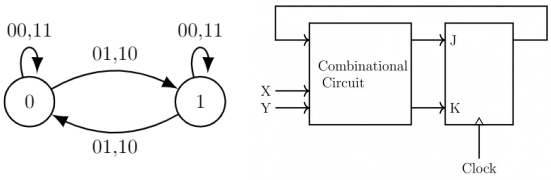
A. 134 B. 133 C. 124 D. 123

gate2005-it digital-logic digital-counter normal

4.12.5 Digital Counter: GATE2008-IT-37

https://gateoverflow.in/3347

Consider the following state diagram and its realization by a JK flip flop



its form characteristic table of JK FF

The combinational circuit generates J and K in terms of x, y and Q.
The Boolean expressions for J and K are :

A. $\overline{x \oplus y}$ and $\overline{x \oplus y}$
B. $\overline{x \oplus y}$ and $x \oplus y$
C. $x \oplus y$ and $\overline{x \oplus y}$
D. $x \oplus y$ and $x \oplus y$

gate2008-it digital-logic boolean-algebra normal digital-counter

4.12.6 Digital Counter: GATE2011-15

https://gateoverflow.in/2117

The minimum number of D flip-flops needed to design a mod-258 counter is

A. 9 B. 8 C. 512 D. 258

gate2011 digital-logic normal digital-counter

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4.12.7 Digital Counter: GATE2014-2-7

https://gateoverflow.in/1959

Let $k = 2^n$. A circuit is built by giving the output of an n-bit binary counter as input to an n-to-2^n bit decoder. This circuit is equivalent to a

A. k-bit binary up counter.
B. k-bit binary down counter.
C. k--bit ring counter.
D. k-bit Johnson counter.

gate2014-2 digital-logic normal digital-counter

4.12.8 Digital Counter: GATE2015-1-20

https://gateoverflow.in/8219

Consider a 4-bit Johnson counter with an initial value of 0000. The counting sequence of this counter is

A. 0, 1, 3, 7, 15, 14, 12, 8, 0
B. 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
C. 0, 2, 4, 6, 8, 10, 12, 14, 0
D. 0, 8, 12, 14, 15, 7, 3, 1, 0

gate2015-1 digital-logic digital-counter easy

4.12.9 Digital Counter: GATE2015-2-7

https://gateoverflow.in/8054

The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0, 0, 1, 1, 2, 2, 3, 3, 0, 0, ...) is _____.

gate2015-2 digital-logic digital-counter normal numerical-answers

4.12.10 Digital Counter: GATE2016-1-8

https://gateoverflow.in/39670

We want to design a synchronous counter that counts the sequence $0-1-0-2-0-3$ and then repeats. The minimum number of J-K flip-flops required to implement this counter is _____.

gate2016-1 digital-logic digital-counter flip-flop normal numerical-answers

4.12.11 Digital Counter: GATE2017-2-42

https://gateoverflow.in/118557

The next state table of a $2-$bit saturating up-counter is given below.

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip-flops. The expressions for T_1 and T_0 are

A. $T_1 = Q_1Q_0, \quad T_0 = \bar{Q}_1\bar{Q}_0$
B. $T_1 = \bar{Q}_1Q_0, \quad T_0 = \bar{Q}_1 + \bar{Q}_0$
C. $T_1 = Q_1 + Q_0, \quad T_0 = \bar{Q}_1\bar{Q}_0$
D. $T_1 = \bar{Q}_1Q_0, \quad T_0 = Q_1 + Q_0$

gate2017-2 digital-logic digital-counter

4.13 Dual Function (1)

4.13.1 Dual Function: GATE2014-2-6

https://gateoverflow.in/1958

The dual of a Boolean function $F(x_1, x_2, \ldots, x_n, +, ., ')$, written as F^D is the same expression as that of F with $+$ and $\cdot$ swapped. F is said to be self-dual if $F = F^D$. The number of self-dual functions with n Boolean variables is

A. 2^n B. 2^{n-1} C. 2^{2^n} D. $2^{2^{n-1}}$

gate2014-2 digital-logic normal dual-function

4.14 Fixed Point Representation (2)

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4.14.1 Fixed Point Representation: GATE2017-1-7

https://gateoverflow.in/118287

The n-bit fixed-point representation of an unsigned real number X uses f bits for the fraction part. Let $i = n - f$. The range of decimal values for X in this representation is

A. 2^{-f} to 2^i
B. 2^{-f} to $\left(2^i - 2^{-f}\right)$
C. 0 to 2^i
D. 0 to $\left(2^i - 2^{-f}\right)$

gate2017-1 digital-logic number-representation fixed-point-representation

4.14.2 Fixed Point Representation: GATE2018-33

https://gateoverflow.in/204107

Consider the unsigned 8-bit fixed point binary number representation, below,

$$b_7\ b_6\ b_5\ b_4\ b_3\ \cdot b_2\ b_1\ b_0$$

where the position of the primary point is between b_3 and b_2 . Assume b_7 is the most significant bit. Some of the decimal numbers listed below **cannot** be represented **exactly** in the above representation:

i. 31.500
ii. 0.875
iii. 12.100
iv. 3.001

Which one of the following statements is true?

A. None of i, ii, iii, iv can be exactly represented
B. Only ii cannot be exactly represented
C. Only iii and iv cannot be exactly represented
D. Only i and ii cannot be exactly represented

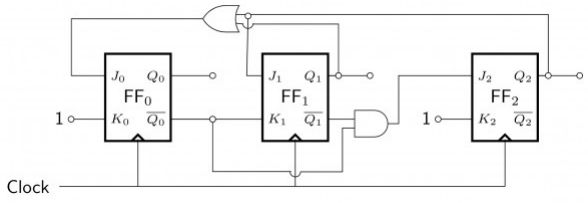
gate2018 digital-logic number-representation fixed-point-representation normal

4.15 Flip Flop (11)

4.15.1 Flip Flop: GATE1990-5-c

https://gateoverflow.in/85400

For the synchronous counter shown in Fig.3, write the truth table of Q_0, Q_1,and Q_2 after each pulse, starting from $Q_0 = Q_1 = Q_2 = 0$ and determine the counting sequence and also the modulus of the counter.

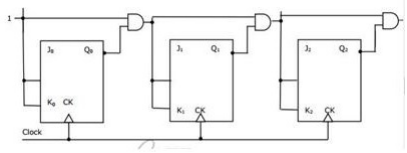


gate1990 descriptive digital-logic flip-flop

4.15.2 Flip Flop: GATE1991-5-c

https://gateoverflow.in/26442

Find the maximum clock frequency at which the counter in the figure below can be operated. Assume that the propagation delay through each flip flop and each AND gate is 10 ns. Also assume that the setup time for the JK inputs of the flip flops is negligible.



gate1991 digital-logic flip-flop

4.15.3 Flip Flop: GATE1992-04-c

https://gateoverflow.in/17408

Design a 3-bit counter using D-flip flops such that not more than one flip-flop changes state between any two consecutive

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states.

gate1994 digital-logic flip-flop

4.15.4 Flip Flop: GATE1992-04c

https://gateoverflow.in/43602

Design a $3-$bit counter using D-flip flops such that not more than one flip-flop changes state between any two consecutive states.

gate1992 normal descriptive digital-logic flip-flop

4.15.5 Flip Flop: GATE2001-11-a

https://gateoverflow.in/752

A sequential circuit takes an input stream of 0's and 1's and produces an output stream of 0's and 1's. Initially it replicates the input on its output until two consecutive 0's are encountered on the input. From then onward, it produces an output stream, which is the bit-wise complement of input stream until it encounters two consecutive 1's, whereupon the process repeats. An example input and output stream is shown below.

The input stream: 101100|01001011 0|11
The desired output 101100|10110100 0|11
J-K master-slave flip-flops are to be used to design the circuit.

Give the state transition diagram

gate2001 digital-logic normal descriptive flip-flop

4.15.6 Flip Flop: GATE2001-11-b

https://gateoverflow.in/203826

A sequential circuit takes an input stream of 0's and 1's and produces an output stream of 0's and 1's. Initially it replicates the input on its output until two consecutive 0's are encountered on the input. From then onward, it produces an output stream, which is the bit-wise complement of input stream until it encounters two consecutive 1's, whereupon the process repeats. An example input and output stream is shown below.

The input stream:	101100 | 01001011	0 | 11
The desired output:	101100 | 10110100	0 | 11

J-K master-slave flip-flops are to be used to design the circuit.

Give the minimized sum-of-product expression for J and K inputs of one of its state flip-flops

gate2001 digital-logic normal descriptive flip-flop

4.15.7 Flip Flop: GATE2004-18, ISRO2007-31

https://gateoverflow.in/1015

In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in

A. $Q = 0, Q' = 1$
B. $Q = 1, Q' = 0$
C. $Q = 1, Q' = 1$
D. Indeterminate states

gate2004 digital-logic easy isro2007 flip-flop

4.15.8 Flip Flop: GATE2007-IT-7

https://gateoverflow.in/3440

Which of the following input sequences for a cross-coupled $R - S$ flip-flop realized with two $NAND$ gates may lead to an oscillation?

A. $11, 00$ B. $01, 10$ C. $10, 01$ D. $00, 11$

gate2007-it digital-logic normal flip-flop

4.15.9 Flip Flop: GATE2015-1-37

https://gateoverflow.in/8287

A positive edge-triggered D flip-flop is connected to a positive edge-triggered JK flip-flop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip-flop is connected to the input of the D flip-flop. Initially, the output of the D flip-flop is set to logic one and the output of the JK flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when the flip-flops are connected to a free-running common clock? Assume that $J = K = 1$ is the toggle mode and $J = K = 0$ is the state holding mode of the JK flip-flops. Both the flip-flops have non-zero propagation delays.

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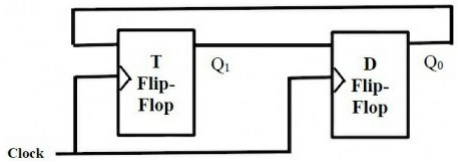
A. 0110110 . . .
B. 0100100 . . .
C. 011101110 . . .
D. 011001100 . . .

gate2015-1 digital-logic flip-flop normal

4.15.10 Flip Flop: GATE2017-1-33

https://gateoverflow.in/118315

Consider a combination of T and D flip-flops connected as shown below. The output of the D flip-flop is connected to the input of the T flip-flop and the output of the T flip-flop is connected to the input of the D flip-flop.



Initially, both Q_0 and Q_1 are set to 1 (before the 1 st clock cycle). The outputs

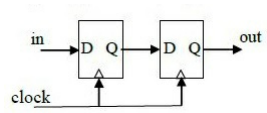
A. Q_1Q_0 after the 3 rd cycle are 11 and after the 4 th cycle are 00 respectively.
B. Q_1Q_0 after the 3 rd cycle are 11 and after the 4 th cycle are 01 respectively.
C. Q_1Q_0 after the 3 rd cycle are 00 and after the 4 th cycle are 11 respectively.
D. Q_1Q_0 after the 3 rd cycle are 01 and after the 4 th cycle are 01 respectively.

gate2017-1 digital-logic flip-flop normal

4.15.11 Flip Flop: GATE2018-22

https://gateoverflow.in/204096

Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered D flip-flops.



The number of states in the state transition diagram of this circuit that have a transition back to the same state on some value of "in" is ____

gate2018 digital-logic flip-flop numerical-answers normal

4.16 Floating Point Representation (8)

4.16.1 Floating Point Representation: GATE1987-1-vii

https://gateoverflow.in/80201

The exponent of a floating-point number is represented in excess-N code so that:

A. The dynamic range is large.
B. The precision is high.
C. The smallest number is represented by all zeros.
D. Overflow is avoided.

gate1987 digital-logic number-representation floating-point-representation

4.16.2 Floating Point Representation: GATE1989-1-vi

https://gateoverflow.in/87053

Consider an excess - 50 representation for floating point numbers with $4BCD$ digit mantissa and $2BCD$ digit exponent in normalised form. The minimum and maximum positive numbers that can be represented are _____ and _____ respectively.

descriptive gate1989 digital-logic number-representation floating-point-representation

4.16.3 Floating Point Representation: GATE1990-1-iv-a

https://gateoverflow.in/83830

A 32-bit floating-point number is represented by a 7-bit signed exponent, and a 24-bit fractional mantissa. The base of the scale factor is 16,

The range of the exponent is _____

gate1990 descriptive digital-logic number-representation floating-point-representation

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4.16.4 Floating Point Representation: GATE1990-1-iv-b

https://gateoverflow.in/203832

A 32-bit floating-point number is represented by a 7-bit signed exponent, and a 24-bit fractional mantissa. The base of the scale factor is 16,

The range of the exponent is _____, if the scale factor is represented in excess-64 format.

gate1990 descriptive digital-logic number-representation floating-point-representation

4.16.5 Floating Point Representation: GATE1997-72

https://gateoverflow.in/19702

Following floating point number format is given

f is a fraction represented by a $6-bit$ mantissa (includes sign bit) in sign magnitude form, e is a $4-bit$ exponent (includes sign hit) in sign magnitude form and $n=(f,e)=f.2^e$ is a floating point number. Let $A=54.75$ in decimal and $B=9.75$ in decimal

a. Represent A and B as floating point numbers in the above format.
b. Show the steps involved in floating point addition of A and B.
c. What is the percentage error (up to one position beyond decimal point) in the addition operation in (b)?

gate1997 digital-logic floating-point-representation normal

4.16.6 Floating Point Representation: GATE2003-43

https://gateoverflow.in/934

The following is a scheme for floating point number representation using 16 bits.

Bit Position	15	14 9	8 0
	s	e	m
	Sign	Exponent	Mantissa

Let s, e, and m be the numbers represented in binary in the sign, exponent, and mantissa fields respectively. Then the floating point number represented is:

$$\begin{cases} (-1)^s \left(1+m\times 2^{-9}\right) 2^{e-31}, & \text{if the exponent } \neq 111111 \\ 0, & \text{otherwise} \end{cases}$$

What is the maximum difference between two successive real numbers representable in this system?

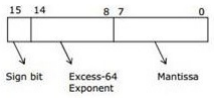
A. 2^{-40} B. 2^{-9} C. 2^{22} D. 2^{31}

gate2003 digital-logic number-representation floating-point-representation normal

4.16.7 Floating Point Representation: GATE2005-85-a

https://gateoverflow.in/1407

Consider the following floating-point format.



Mantissa is a pure fraction in sign-magnitude form.

The decimal number 0.239×2^{13} has the following hexadecimal representation (without normalization and rounding off):

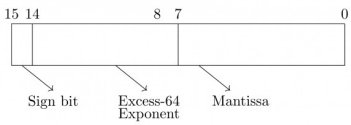
A. 0D 24 B. 0D 4D C. 4D 0D D. 4D 3D

gate2005 digital-logic number-representation floating-point-representation normal

4.16.8 Floating Point Representation: GATE2005-85-b

https://gateoverflow.in/82139

Consider the following floating-point format.



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Mantissa is a pure fraction in sign-magnitude form.

The normalized representation for the above format is specified as follows. The mantissa has an implicit 1 preceding the binary (radix) point. Assume that only $0's$ are padded in while shifting a field.

The normalized representation of the above number (0.239×2^{13}) is:

A. $0A\ 20$ B. $11\ 34$ C. $49\ D0$ D. $4A\ E8$

gate2005 digital-logic number-representation floating-point-representation normal

4.17 Functional Completeness (4)

4.17.1 Functional Completeness: GATE1989-4-iii

https://gateoverflow.in/87883

Provide short answers to the following questions:

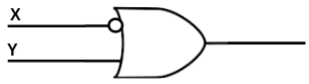
Show that {NOR} is a functionally complete set of Boolean operations.

gate1989 descriptive digital-logic functional-completeness

4.17.2 Functional Completeness: GATE1998-5

https://gateoverflow.in/1696

The implication gate, shown below has two inputs (x and y); the output is 1 except when $x = 1$ and $y = 0$, realize $f = \bar{x}y + x\bar{y}$ using only four implication gates.



Show that the implication gate is functionally complete.

gate1998 digital-logic functional-completeness descriptive

4.17.3 Functional Completeness: GATE1999-2.9

https://gateoverflow.in/1487

Which of the following sets of component(s) is/are sufficient to implement any arbitrary Boolean function?

A. XOR gates, NOT gates
B. 2 to 1 multiplexers
C. AND gates, XOR gates
D. Three-input gates that output $(A.B) + C$ for the inputs A, B and C.

gate1999 digital-logic normal functional-completeness

4.17.4 Functional Completeness: GATE2008-IT-1

https://gateoverflow.in/3222

A set of Boolean connectives is functionally complete if all Boolean functions can be synthesized using those. Which of the following sets of connectives is NOT functionally complete?

A. EX-NOR B. implication, negation C. OR, negation D. NAND

gate2008-it digital-logic easy functional-completeness

4.18 Functions (1)

4.18.1 Functions: GATE1987-1-II

https://gateoverflow.in/80032

The total number of Boolean functions which can be realised with four variables is:

A. 4 B. 17 C. 256 D. $65,536$

gate1987 digital-logic boolean-algebra functions permutation-and-combination

4.19 Gray Code (1)

4.19.1 Gray Code: TIFR2017-B-8

https://gateoverflow.in/95703

For any natural number n, an ordering of all binary strings of length n is a Gray code if it starts with 0^n, and any successive strings in the ordering differ in exactly one bit (the first and last string must also differ by one bit). Thus, for $n = 3$, the ordering (000, 100, 101, 111, 110, 010, 011, 001) is a Gray code. Which of the following must be TRUE for all Gray

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codes over strings of length n?

A. the number of possible Gray codes is even
B. the number of possible Gray codes is odd
C. In any Gray code, if two strings are separated by k other strings in the ordering, then they must differ in exactly $k+1$ bits
D. In any Gray code, if two strings are separated by k other strings in the ordering, then they must differ in exactly k bits
E. none of the above

tifr2017 digital-logic binary-codes gray-code

4.20 Ieee Representation (5)

4.20.1 Ieee Representation: GATE2008-4

https://gateoverflow.in/402

In the IEEE floating point representation the hexadecimal value $0\text{x}00000000$ corresponds to

A. The normalized value 2^{-127}
B. The normalized value 2^{-126}
C. The normalized value $+0$
D. The special value $+0$

gate2008 digital-logic floating-point-representation ieee-representation easy

4.20.2 Ieee Representation: GATE2008-IT-7

https://gateoverflow.in/3267

The following bit pattern represents a floating point number in IEEE 754 single precision format

1 10000011 10100000000000000000000

The value of the number in decimal form is

A. -10 B. -13 C. -26 D. None of the above

gate2008-it digital-logic number-representation floating-point-representation ieee-representation normal

4.20.3 Ieee Representation: GATE2012-7

https://gateoverflow.in/39

The decimal value 0.5 in IEEE single precision floating point representation has

A. fraction bits of $000\ldots000$ and exponent value of 0
B. fraction bits of $000\ldots000$ and exponent value of -1
C. fraction bits of $100\ldots000$ and exponent value of 0
D. no exact representation

gate2012 digital-logic normal number-representation ieee-representation

4.20.4 Ieee Representation: GATE2014-2-45

https://gateoverflow.in/2011

The value of a float type variable is represented using the single-precision 32-bit floating point format of $IEEE-754$ standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for the mantissa. A float type variable X is assigned the decimal value of -14.25. The representation of X in hexadecimal notation is

A. $C1640000H$ B. $416C0000H$ C. $41640000H$ D. $C16C0000H$

gate2014-2 digital-logic number-representation normal ieee-representation

4.20.5 Ieee Representation: GATE2017-2-12

https://gateoverflow.in/118434

Given the following binary number in 32-bit (single precision) $IEEE-754$ format :

$$00111110011011010000000000000000$$

The decimal value closest to this floating-point number is :

A. $1.45*10^{1}$ B. $1.45*10^{-1}$ C. $2.27*10^{-1}$ D. $2.27*10^{1}$

gate2017-2 digital-logic number-representation floating-point-representation ieee-representation

4.21 K Map (19)

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4.21.1 K Map: GATE1987-16-a

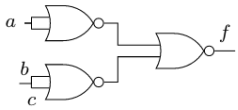
https://gateoverflow.in/82698

A Boolean function f is to be realized only by NOR gates. Its $K-map$ is given below:

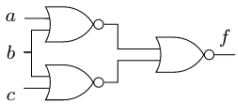
c \ ab	00	01	11	10
0	0	0	1	1
1	0	1	1	1

The realization is

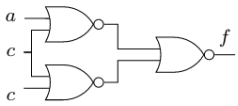
A.



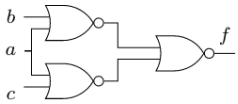
B.



C.



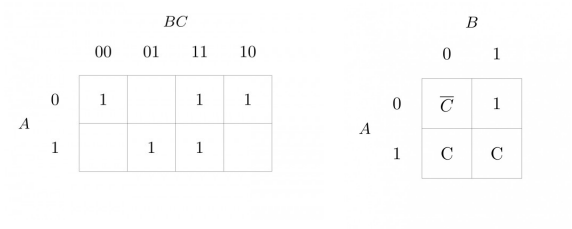
D.



gate1987 digital-logic k-map

4.21.2 K Map: GATE1988-3a-b

https://gateoverflow.in/94358



The Karnaugh map of a function of (A, B, C) is shown on the left hand side of the above figure.

The reduced form of the same map is shown on the right hand side, in which the variable C is entered in the map itself. Discuss,

a. The methodology by which the reduced map has been derived and
b. the rules (or steps) by which the boolean function can be derived from the entries in the reduced map.

gate1988 descriptive digital-logic k-map

4.21.3 K Map: GATE1992-01-i

https://gateoverflow.in/545

The Boolean function in sum of products form where K-map is given below (figure) is _____

B \ C	0	1
0	1	0
1	$\overline{A}$	A

gate1992 digital-logic k-map normal

4.21.4 K Map: GATE1995-15-a

https://gateoverflow.in/2651

Implement a circuit having the following output expression using an inverter and a nand gate

$$Z = \overline{A} + \overline{B} + C$$

gate1995 digital-logic k-map normal descriptive

4.21.5 K Map: GATE1995-15-b

https://gateoverflow.in/203837

What is the equivalent minimal Boolean expression (in sum of products form) for the Karnaugh map given below?

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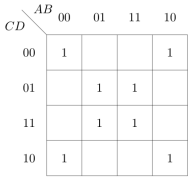
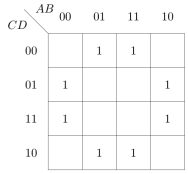


gate1995 digital-logic k-map normal

4.21.6 K Map: GATE1996-2.24

https://gateoverflow.in/2753

What is the equivalent Boolean expression in product-of-sums form for the Karnaugh map given in Fig



A. $B\overline{D} + \overline{B}D$

B. $(B + \overline{C} + D)(\overline{B} + C + \overline{D})$

C. $(B + D)(\overline{B} + \overline{D})$

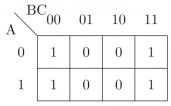
D. $(B + \overline{D})(\overline{B} + D)$

gate1996 digital-logic k-map easy

4.21.7 K Map: GATE1998-2.7

https://gateoverflow.in/1679

The function represented by the Karnaugh map given below is



A. $A.B$

B. $AB + BC + CA$

C. $\overline{B \oplus C}$

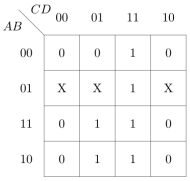
D. $A.BC$

gate1998 digital-logic k-map normal

4.21.8 K Map: GATE1999-1.8

https://gateoverflow.in/1461

Which of the following functions implements the Karnaugh map shown below?



A. $\bar{A}B + CD$

B. $D(C + A)$

C. $AD + \bar{A}B$

D. $(C + D)(\bar{C} + D) + (A + B)$

gate1999 digital-logic k-map easy

4.21.9 K Map: GATE2000-2.11

https://gateoverflow.in/658

Which functions does NOT implement the Karnaugh map given below?

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xy \ wz	00	01	11	10
00	0	X	0	0
01	0	X	1	1
11	1	1	1	1
10	0	X	0	0

A. $(w+x)y$
B. $xy+yw$
C. $(w+x)(\bar{w}+y)(\bar{x}+y)$
D. None of the above

gate2000 digital-logic k-map normal

4.21.10 K Map: GATE2001-1.11

https://gateoverflow.in/704

Given the following karnaugh map, which one of the following represents the minimal Sum-Of-Products of the map?

yz \ wx	00	01	11	10
00	0	X	0	X
01	X	1	X	1
11	0	X	1	0
10	0	1	X	0

A. $XY+Y'Z$ B. $WX'Y'+XY+XZ$ C. $W'X+Y'Z+XY$ D. $XZ+Y$

gate2001 k-map digital-logic normal

4.21.11 K Map: GATE2002-1.12

https://gateoverflow.in/816

Minimum sum of product expression for $f(w,x,y,z)$ shown in Karnaugh-map below

yz \ wx	00	01	11	10
00	0	1	1	0
01	X	0	0	1
11	X	0	0	1
10	0	1	1	X

A. $xz+y'z$ B. $xz'+zx'$ C. $x'y+zx'$ D. None of the above

gate2002 digital-logic k-map normal

4.21.12 K Map: GATE2003-45

https://gateoverflow.in/936

The literal count of a Boolean expression is the sum of the number of times each literal appears in the expression. For example, the literal count of $(xy+xz')$ is 4. What are the minimum possible literal counts of the product-of-sum and sum-of-product representations respectively of the function given by the following Karnaugh map? Here, X denotes "don't care"

xy \ zw	00	01	11	10
00	X	1	0	1
01	0	1	X	0
11	1	X	X	0
10	X	0	0	X

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A. $(11, 9)$ B. $(9, 13)$ C. $(9, 10)$ D. $(11, 11)$

gate2003 digital-logic k-map normal

4.21.13 K Map: GATE2006-IT-35

https://gateoverflow.in/3574

The boolean function for a combinational circuit with four inputs is represented by the following Karnaugh map.

RS \ PQ	00	01	11	10
00	1	0	0	1
01	0	0	1	1
11	1	1	1	0
10	1	0	0	1

Only the top leftmost and bottom rightmost 1s have no alternate groupings. So, they form the essential prime implicants.

Which of the product terms given below is an essential prime implicant of the function?

A. QRS B. PQS C. PQ'S' D. Q'S'

gate2006-it digital-logic k-map normal

4.21.14 K Map: GATE2007-IT-78

https://gateoverflow.in/3530

Consider the following expression

$a\bar{d} + \bar{a}\bar{c} + b\bar{c}d$

Which of the following Karnaugh Maps correctly represents the expression?

A.

ab \ cd	00	01	11	10
00	X	X		
01	X	X		
11	X	X		X
10	X			X

B.

ab \ cd	00	01	11	10
00	X	X		
01	X			
11	X	X		X
10	X	X		X

C.

ab \ cd	00	01	11	10
00	X	X		
01	X	X		X
11	X	X		X
10	X			X

D.

ab \ cd	00	01	11	10
00	X	X		
01	X	X		X
11	X	X		X
10	X		X	X

gate2007-it digital-logic k-map normal

4.21.15 K Map: GATE2007-IT-79

https://gateoverflow.in/3531

Consider the following expression

$a\bar{d} + \bar{a}\bar{c} + b\bar{c}d$

Which of the following expressions does not correspond to the Karnaugh Map obtained for the given expression?

A. $\bar{c}\bar{d} + a\bar{d} + ab\bar{c} + \bar{a}\bar{c}d$
B. $\bar{a}\bar{c} + \bar{c}\bar{d} + a\bar{d} + ab\bar{c}d$
C. $\bar{a}\bar{c} + a\bar{d} + ab\bar{c} + \bar{c}d$
D. $\bar{b}\bar{c}\bar{d} + ac\bar{d} + \bar{a}\bar{c} + ab\bar{c}$

gate2007-it digital-logic k-map normal

4.21.16 K Map: GATE2008-5

https://gateoverflow.in/403

In the Karnaugh map shown below, X denotes a don't care term. What is the minimal form of the function represented by the Karnaugh map?

cd \ ab	00	01	11	10
00	1	1		1
01	X			
11	X			
10	1	1		X

A. $\bar{b}.\bar{d} + \bar{a}.\bar{d}$
B. $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.b.\bar{d}$
C. $\bar{b}.\bar{d} + \bar{a}.b.\bar{d}$
D. $\bar{a}.\bar{b} + \bar{b}.\bar{d} + \bar{a}.\bar{d}$

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gate2008 digital-logic k-map easy

4.21.17 K Map: GATE2012-30

https://gateoverflow.in/1615

What is the minimal form of the Karnaugh map shown below? Assume that X denotes a don't care term

cd \ ab	00	01	11	10
00	1	X	X	1
01	X			1
11				
10	1			X

A. $\bar{b}\bar{d}$
B. $\bar{b}\bar{d}+\bar{b}\bar{c}$
C. $\bar{b}\bar{d}+a\bar{b}\bar{c}d$
D. $\bar{b}\bar{d}+\bar{b}\bar{c}+\bar{c}\bar{d}$

gate2012 digital-logic k-map easy

4.21.18 K Map: GATE2017-1-21

https://gateoverflow.in/118301

Consider the Karnaugh map given below, where X represents *"don't care"* and blank represents 0.

dc \ ba	00	01	11	10
00		X	X	
01	1			X
11	1			1
10		X	X	

Assume for all inputs (a, b, c, d), the respective complements $\left(\bar{a}, \bar{b}, \bar{c}, \bar{d}\right)$ are also available. The above logic is implemented using 2-input NOR gates only. The minimum number of gates required is _____ .

gate2017-1 digital-logic k-map numerical-answers normal

4.21.19 K Map: GATE2019-30

https://gateoverflow.in/302818

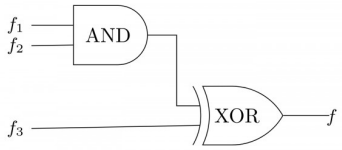
Consider three 4-variable functions f_1, f_2, and f_3, which are expressed in sum-of-minterms as

$f_1 = \Sigma(0, 2, 5, 8, 14)$,

$f_2 = \Sigma(2, 3, 6, 8, 14, 15)$,

$f_3 = \Sigma(2, 7, 11, 14)$

For the following circuit with one AND gate and one XOR gate the output function f can be expressed as:



A. $\Sigma(7, 8, 11)$
B. $\Sigma(2, 7, 8, 11, 14)$
C. $\Sigma(2, 14)$
D. $\Sigma(0, 2, 3, 5, 6, 7, 8, 11, 14, 15)$

gate2019 digital-logic k-map digital-circuits

4.22 Memory Interfacing (3)

4.22.1 Memory Interfacing: GATE1995-2.2

https://gateoverflow.in/2614

The capacity of a memory unit is defined by the number of words multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of $4K \times 16$?

A. 10 address, 16 data lines
B. 11 address, 8 data lines

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C. 12 address, 16 data lines
D. 12 address, 12 data lines

gate1995 digital-logic memory-interfacing normal

4.22.2 Memory Interfacing: GATE2005-IT-9

https://gateoverflow.in/3754

A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec . What percentage of the memory cycle time is used for refreshing?

A. 10 B. 6.4 C. 1 D. 0.64

gate2005-it digital-logic memory-interfacing normal

4.22.3 Memory Interfacing: GATE2010-7

https://gateoverflow.in/2178

The main memory unit with a capacity of 4 megabytes is built using $1M\times$ 1-bit DRAM chips. Each DRAM chip has 1K rows of cells with $1K$ cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is

A. 100 nanoseconds
B. 100×2^{10} nanoseconds
C. 100×2^{20} nanoseconds
D. 3200×2^{20} nanoseconds

gate2010 digital-logic memory-interfacing normal

4.23 Min No Gates (4)

4.23.1 Min No Gates: GATE2000-9

https://gateoverflow.in/680

Design a logic circuit to convert a single digit BCD number to the number modulo six as follows (Do not detect illegal input):

A. Write the truth table for all bits. Label the input bits $I_1, I_2, \ldots$ with I_1 as the least significant bit. Label the output bits $R_1, R_2 \ldots$ with R_1 as the least significant bit. Use 1 to signify truth.
B. Draw one circuit for each output bit using, ***altogether***, two two-input AND gates, one two-input OR gate and two NOT gates.

gate2000 digital-logic min-no-gates descriptive

4.23.2 Min No Gates: GATE2004-58

https://gateoverflow.in/1053

A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001, …, 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and outputs 1 if the digit ≥ 5, and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required?

A. 2 B. 3 C. 4 D. 5

gate2004 digital-logic normal min-no-gates

4.23.3 Min No Gates: GATE2004-IT-8

https://gateoverflow.in/3649

What is the minimum number of NAND gates required to implement a 2-input EXCLUSIVE-OR function without using any other logic gate?

A. 2 B. 4 C. 5 D. 6

gate2004-it digital-logic min-no-gates normal

4.23.4 Min No Gates: GATE2009-6

https://gateoverflow.in/1298

What is the minimum number of gates required to implement the Boolean function $(AB+C)$ if we have to use only 2-input NOR gates?

A. 2 B. 3 C. 4 D. 5

gate2009 digital-logic min-no-gates normal

4.24 Min Product Of Sums (1)

4.24.1 Min Product Of Sums: GATE2017-2-28

https://gateoverflow.in/118370

Given $f(w,x,y,z) = \Sigma_m(0,1,2,3,7,8,10) + \Sigma_d(5,6,11,15)$; where d represents the '*don't-care*' condition in

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Karnaugh maps. Which of the following is a minimum product-of-sums (POS) form of $f(w,x,y,z)$?

A. $f=(\bar{w}+\bar{z})(\bar{x}+z)$
B. $f=(\bar{w}+z)(x+z)$
C. $f=(w+z)(\bar{x}+z)$
D. $f=(w+\bar{z})(\bar{x}+z)$

gate2017-2 digital-logic min-product-of-sums

4.25 Min Sum Of Products Form (12)

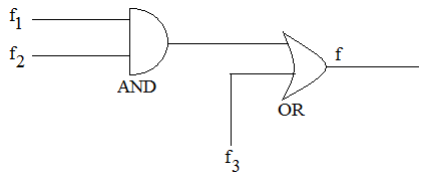
4.25.1 Min Sum Of Products Form: GATE1988-2-v

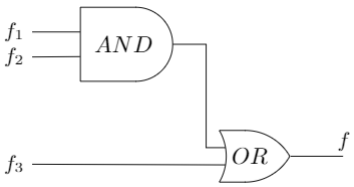
https://gateoverflow.in/91685

Three switching functions $f_1,\ f_2$ and f_3 are expressed below as sum of minterms.

- $f_1(w,x,y,z)=\sum 0,1,2,3,5,12$
- $f_2(w,x,y,z)=\sum 0,1,2,10,13,14,15$
- $f_3(w,x,y,z)=\sum 2,4,5,8$

Express the function f realised by the circuit shown in the below figure as the sum of minterms (in decimal notation).





gate1988 descriptive digital-logic easy circuit-output min-sum-of-products-form

4.25.2 Min Sum Of Products Form: GATE1991-5-b

https://gateoverflow.in/26437

Find the minimum sum of products form of the logic function $f(A,B,C,D)=\Sigma m(0,2,8,10,15)+\Sigma d(3,11,12,14)$ where m and d represent minterm and don't care term respectively.

gate1991 digital-logic min-sum-of-products-form

4.25.3 Min Sum Of Products Form: GATE1997-71

https://gateoverflow.in/19701

Let $f=(\bar{w}+y)(\bar{x}+y)(w+\bar{x}+z)(\bar{w}+z)(\bar{x}+z)$

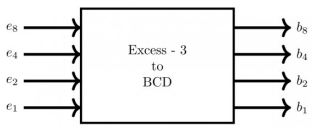
A. Express f as the minimal sum of products. Write only the answer.
B. If the output line is stuck at 0, for how many input combinations will the value of f be correct?

gate1997 digital-logic min-sum-of-products-form

4.25.4 Min Sum Of Products Form: GATE2001-10

https://gateoverflow.in/751

a. Is the 3-variable function $f=\Sigma(0,1,2,4)$ its self-dual? Justify your answer.
b. Give a minimal product-of-sum form of the b output of the following excess-3 to BCD converter.



gate2001 digital-logic normal descriptive min-sum-of-products-form

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4.25.5 Min Sum Of Products Form: GATE2005-18

https://gateoverflow.in/1354

The switching expression corresponding to $f(A, B, C, D) = \Sigma(1, 4, 5, 9, 11, 12)$ is:

A. $BC'D' + A'C'D + AB'D$
B. $ABC' + ACD + B'C'D$
C. $ACD' + A'BC' + AC'D'$
D. $A'BD + ACD' + BCD'$

gate2005 digital-logic normal min-sum-of-products-form

4.25.6 Min Sum Of Products Form: GATE2007-9

https://gateoverflow.in/1207

Consider the following Boolean function of four variables:

$$f(w, x, y, z) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14)$$

The function is

A. independent of one variables.
B. independent of two variables.
C. independent of three variables.
D. dependent on all variables

gate2007 digital-logic normal min-sum-of-products-form

4.25.7 Min Sum Of Products Form: GATE2008-IT-8

https://gateoverflow.in/3268

Consider the following Boolean function of four variables
$f(A, B, C, D) = \Sigma(2, 3, 6, 7, 8, 9, 10, 11, 12, 13)$
The function is

A. independent of one variable
B. independent of two variables
C. independent of three variable
D. dependent on all the variables

gate2008-it digital-logic normal min-sum-of-products-form

4.25.8 Min Sum Of Products Form: GATE2011-14

https://gateoverflow.in/2116

The simplified SOP (Sum of Product) from the Boolean expression

$$(P + \bar{Q} + \bar{R}).(P + \bar{Q} + R).(P + Q + \bar{R})$$

is

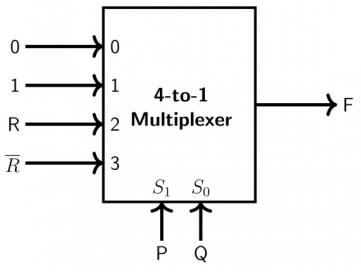
A. $(\bar{P}.Q + \bar{R})$ B. $(P + \bar{Q}.\bar{R})$ C. $(\bar{P}.Q + R)$ D. $(P.Q + R)$

gate2011 digital-logic normal min-sum-of-products-form

4.25.9 Min Sum Of Products Form: GATE2014-1-45

https://gateoverflow.in/1923

Consider the 4-to-1 multiplexer with two select lines S_1 and S_0 given below



The minimal sum-of-products form of the Boolean expression for the output F of the multiplexer is

A. $\bar{P}Q + Q\bar{R} + P\bar{Q}R$
B. $\bar{P}Q + \bar{P}Q\bar{R} + PQ\bar{R} + P\bar{Q}R$
C. $\bar{P}QR + \bar{P}Q\bar{R} + Q\bar{R} + P\bar{Q}R$
D. $PQ\bar{R}$

gate2014-1 digital-logic normal multiplexer min-sum-of-products-form

4.25.10 Min Sum Of Products Form: GATE2014-1-7

https://gateoverflow.in/1764

Consider the following Boolean expression for F:

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$F(P,Q,R,S) = PQ + \bar{P}QR + \bar{P}Q\bar{R}S$

The minimal sum−of−products form of F is

A. $PQ + QR + QS$
B. $P + Q + R + S$
C. $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$
D. $\bar{P}R + \bar{R}\bar{P}S + P$

gate2014-1 digital-logic normal min-sum-of-products-form

4.25.11 Min Sum Of Products Form: GATE2014-3-7

https://gateoverflow.in/2041

Consider the following minterm expression for F:

$$F(P,Q,R,S) = \sum 0, 2, 5, 7, 8, 10, 13, 15$$

The minterms 2, 7, 8 and 13 are 'do not care' terms. The minimal sum-of-products form for F is

A. $Q\bar{S} + \bar{Q}S$
B. $\bar{Q}\bar{S} + QS$
C. $\bar{Q}\bar{R}\bar{S} + \bar{Q}R\bar{S} + Q\bar{R}S + QRS$
D. $\bar{P}\bar{Q}\bar{S} + \bar{P}QS + PQS + P\bar{Q}\bar{S}$

gate2014-3 digital-logic min-sum-of-products-form normal

4.25.12 Min Sum Of Products Form: GATE2018-49

https://gateoverflow.in/204124

Consider the minterm list form of a Boolean function F given below.

$$F(P,Q,R,S) = \Sigma m(0,2,5,7,9,11) + d(3,8,10,12,14)$$

Here, m denotes a minterm and d denotes a don't care term. The number of essential prime implicants of tte function F is ___

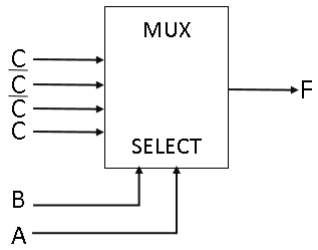
gate2018 digital-logic min-sum-of-products-form numerical-answers

4.26 Multiplexer (11)

4.26.1 Multiplexer: GATE1987-1-IV

https://gateoverflow.in/80193

The output F of the below multiplexer circuit can be represented by



A. $AB + B\bar{C} + \bar{C}A + \bar{B}\bar{C}$
B. $A \oplus B \oplus C$
C. $A \oplus B$
D. $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$

gate1987 digital-logic circuit-output multiplexer

4.26.2 Multiplexer: GATE1990-5-b

https://gateoverflow.in/85398

Show with the help of a block diagram how the Boolean function :

$f = AB + BC + CA$

can be realised using only a $4:1$ multiplexer.

gate1990 descriptive digital-logic multiplexer

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4.26.3 Multiplexer: GATE1992-04-b

https://gateoverflow.in/17407

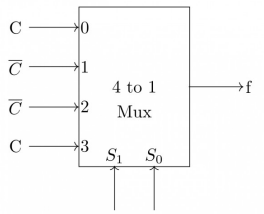
A priority encoder accepts three input signals $(\mathrm{A}, \mathrm{B} \text{ and } \mathrm{C})$ and produces a two-bit output (X_1, X_0) corresponding to the highest priority active input signal. Assume A has the highest priority followed by B and C has the lowest priority. If none of the inputs are active the output should be 00, design the priority encoder using $4:1$ multiplexers as the main components.

gate1994 digital-logic multiplexer descriptive

4.26.4 Multiplexer: GATE1996-2.22

https://gateoverflow.in/2751

Consider the circuit in figure. f implements



A. $\overline{A}\overline{B}C + \overline{A}B\overline{C} + ABC$
B. $A + B + C$
C. $A \oplus B \oplus C$
D. $AB + BC + CA$

gate1996 digital-logic circuit-output easy multiplexer

4.26.5 Multiplexer: GATE1998-1.14

https://gateoverflow.in/1651

A multiplexer with a $4 - bit$ data select input is a

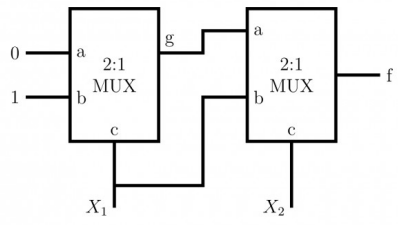
A. $4:1$ multiplexer
B. $2:1$ multiplexer
C. $16:1$ multiplexer
D. $8:1$ multiplexer

gate1998 digital-logic multiplexer easy

4.26.6 Multiplexer: GATE2001-2.11

https://gateoverflow.in/729

Consider the circuit shown below. The output of a $2:1$ MUX is given by the function $(ac' + bc)$.



Which of the following is true?

A. $f = X_1' + X_2$
B. $f = X_1'X_2 + X_1X_2'$
C. $f = X_1X_2 + X_1'X_2'$
D. $f = X_1 + X_2'$

gate2001 digital-logic normal multiplexer

4.26.7 Multiplexer: GATE2004-60

https://gateoverflow.in/1055

Consider a multiplexer with X and Y as data inputs and Z the as the control input. $Z = 0$ selects input X, and $Z = 1$ selects input Y. What are the connections required to realize the 2-variable Boolean function $f = T + R$, without using any additional hardware?

A. R to X, 1 to Y, T to Z
B. T to X, R to Y, T to Z
C. T to X, R to Y, 0 to Z
D. R to X, 0 to Y, T to Z

gate2004 digital-logic normal multiplexer

4.26.8 Multiplexer: GATE2005-IT-48

https://gateoverflow.in/3809

The circuit shown below implements a 2-input NOR gate using two $2 - 4$ MUX (control signal 1 selects the upper input). What are the values of signals x, y and z?

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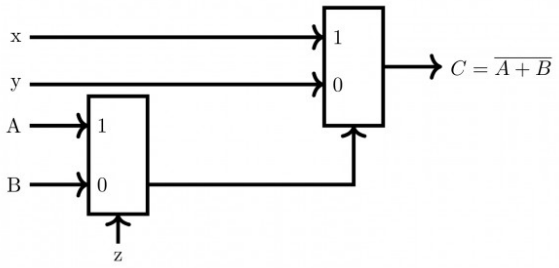


A. $1, 0, B$ B. $1, 0, A$ C. $0, 1, B$ D. $0, 1, A$

gate2005-it digital-logic normal multiplexer

4.26.9 Multiplexer: GATE2007-34

https://gateoverflow.in/1232

Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?

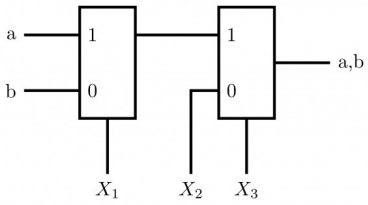
A. 2^n line to 1 line
B. 2^{n+1} line to 1line
C. 2^{n-1} line to 1line
D. 2^{n-2} line to 1line

gate2007 digital-logic normal multiplexer

4.26.10 Multiplexer: GATE2007-IT-8

https://gateoverflow.in/3441

The following circuit implements a two-input AND gate using two $2-1$ multiplexers.



What are the values of X_1, X_2, X_3?

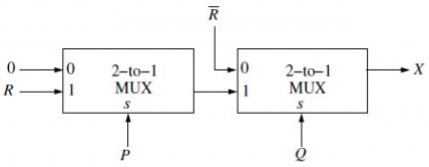
A. $X_1 = b, X_2 = 0, X_3 = a$
B. $X_1 = b, X_2 = 1, X_3 = b$
C. $X_1 = a, X_2 = b, X_3 = 1$
D. $X_1 = a, X_2 = 0, X_3 = b$

gate2007-it digital-logic normal multiplexer

4.26.11 Multiplexer: GATE2016-1-30

https://gateoverflow.in/39722

Consider the two cascade 2 to 1 multiplexers as shown in the figure .



The minimal sum of products form of the output X is

A. $\overline{P}\,\overline{Q} + PQR$
B. $\overline{P}\,Q + QR$
C. $PQ + \overline{P}\,\overline{Q}R$
D. $\overline{Q}\,\overline{R} + PQR$

gate2016-1 digital-logic multiplexer normal

4.27 Number Representation (51)

4.27.1 Number Representation: GATE1988-2-vi

https://gateoverflow.in/91687

Define the value of r in the following: $\sqrt{(41)_r} = (7)_{10}$

gate1988 digital-logic normal number-representation numerical-answers

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4.27.2 Number Representation: GATE1990-1-viii

https://gateoverflow.in/87055

The condition for overflow in the addition of two $2's$ complement numbers in terms of the carry generated by the two most significant bits is _____.

gate1990 descriptive digital-logic number-representation

4.27.3 Number Representation: GATE1991-01-iii

https://gateoverflow.in/500

Consider the number given by the decimal expression:

$$16^3 * 9 + 16^2 * 7 + 16 * 5 + 3$$

The number of $1's$ in the unsigned binary representation of the number is _____

gate1991 digital-logic number-representation normal

4.27.4 Number Representation: GATE1991-01-v

https://gateoverflow.in/503

When two $4 - bit$ numbers $A = a_3a_2a_1a_0$ and $B = b_3b_2b_1b_0$ are multiplied, the bit c_1 of the product C is given by _____

gate1991 digital-logic normal number-representation

4.27.5 Number Representation: GATE1992-4-a

https://gateoverflow.in/583

Consider addition in two's complement arithmetic. A carry from the most significant bit does not always correspond to an overflow. Explain what is the condition for overflow in two's complement arithmetic.

gate1992 digital-logic normal number-representation

4.27.6 Number Representation: GATE1993-6.5

https://gateoverflow.in/2286

Convert the following numbers in the given bases into their equivalents in the desired bases:

A. $(110.101)_2 = (x)_{10}$
B. $(1118)_{10} = (y)_H$

gate1993 digital-logic number-representation normal

4.27.7 Number Representation: GATE1994-2.7

https://gateoverflow.in/2474

Consider n-bit (including sign bit) 2's complement representation of integer numbers. The range of integer values, N, that can be represented is _____ $\leq N \leq$_____ .

gate1994 digital-logic number-representation easy

4.27.8 Number Representation: GATE1995-18

https://gateoverflow.in/2655

The following is an incomplete Pascal function to convert a given decimal integer (in the range -8 to $+7$) into a binary integer in $2's$ complement representation. Determine the expressions A, B, C that complete program.

```
function TWOSCOMP (N:integer):integer;
    var
    REM, EXPONENT:integer;
    BINARY :integer;
    begin
        if(N>=-8) and (N<=+7) then
        begin
            if N<0 then
                N:=A;
            BINARY:=0;
            EXPONENT:=1;
            while N<>0 do
            begin
                REM:=N mod 2;
                BIANRY:=BINARY + B*EXPONENT;
```

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```
                EXPONENT:=EXPONENT*10;
                N:=C
            end
            TWOSCOMP:=BINARY
        end
    end;
```

gate1995 digital-logic number-representation normal

4.27.9 Number Representation: GATE1995-2.12, ISRO2015-9

https://gateoverflow.in/2624

The number of 1's in the binary representation of $(3 * 4096 + 15 * 256 + 5 * 16 + 3)$ are:

A. 8 B. 9 C. 10 D. 12

gate1995 digital-logic number-representation normal isro2015

4.27.10 Number Representation: GATE1996-1.25

https://gateoverflow.in/2729

Consider the following floating-point number representation.

31 24	23 0
Exponent	Mantissa

The exponent is in $2's$ complement representation and the mantissa is in the sign-magnitude representation. The range of the magnitude of the normalized numbers in this representation is

A. 0 to 1 B. 0.5 to 1 C. 2^{-23} to 0.5 D. 0.5 to $\left(1-2^{-23}\right)$

gate1996 digital-logic number-representation normal

4.27.11 Number Representation: GATE1997-5.4

https://gateoverflow.in/2255

Given $\sqrt{(224)_r} = (13)_r$.

The value of the radix r is:

A. 10 B. 8 C. 5 D. 6

gate1997 digital-logic number-representation normal

4.27.12 Number Representation: GATE1998-1.17

https://gateoverflow.in/1654

The octal representation of an integer is $(342)_8$. If this were to be treated as an eight-bit integer in an 8085 based computer, its decimal equivalent is

A. 226 B. -98 C. 76 D. -30

gate1998 digital-logic number-representation normal 8085

4.27.13 Number Representation: GATE1998-2.20

https://gateoverflow.in/1693

Suppose the domain set of an attribute consists of signed four digit numbers. What is the percentage of reduction in storage space of this attribute if it is stored as an integer rather than in character form?

A. 80% B. 20% C. 60% D. 40%

gate1998 digital-logic number-representation normal

4.27.14 Number Representation: GATE1999-2.17

https://gateoverflow.in/1495

Zero has two representations in

A. Sign-magnitude
B. $2's$ complement
C. $1's$ complement
D. None of the above

gate1999 digital-logic number-representation easy

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4.27.15 Number Representation: GATE2000-1.6

https://gateoverflow.in/629

The number 43 in $2's$ complement representation is

A. 01010101 B. 11010101 C. 00101011 D. 10101011

gate2000 digital-logic number-representation easy

4.27.16 Number Representation: GATE2000-2.14

https://gateoverflow.in/661

Consider the values of A = 2.0 x 10^{30}, B = -2.0 x 10^{30}, C = 1.0, and the sequence

```
X:= A + B          Y:= A + C
X:= X + C          Y:= Y + B
```

executed on a computer where floating point numbers are represented with 32 bits. The values for X and Y will be

A. $X = 1.0, Y = 1.0$
B. $X = 1.0, Y = 0.0$
C. $X = 0.0, Y = 1.0$
D. $X = 0.0, Y = 0.0$

gate2000 digital-logic number-representation normal

4.27.17 Number Representation: GATE2001-2.10

https://gateoverflow.in/728

The $2's$ complement representation of $(-539)_{10}$ in hexadecimal is

A. ABE B. DBC C. $DE5$ D. $9E7$

gate2001 digital-logic number-representation easy

4.27.18 Number Representation: GATE2002-1.14

https://gateoverflow.in/818

The decimal value 0.25

A. is equivalent to the binary value 0.1
B. is equivalent to the binary value 0.01
C. is equivalent to the binary value 0.00111
D. cannot be represented precisely in binary

gate2002 digital-logic number-representation easy

4.27.19 Number Representation: GATE2002-1.15

https://gateoverflow.in/819

The $2's$ complement representation of the decimal value -15 is

A. 1111 B. 11111 C. 111111 D. 10001

gate2002 digital-logic number-representation easy

4.27.20 Number Representation: GATE2002-1.16

https://gateoverflow.in/821

Sign extension is a step in

A. floating point multiplication
B. signed 16 bit integer addition
C. arithmetic left shift
D. converting a signed integer from one size to another

gate2002 digital-logic easy number-representation

4.27.21 Number Representation: GATE2002-1.21

https://gateoverflow.in/826

In $2's$ complement addition, overflow

A. is flagged whenever there is carry from sign bit addition
B. cannot occur when a positive value is added to a negative value
C. is flagged when the carries from sign bit and previous bit match
D. None of the above

gate2002 digital-logic number-representation normal

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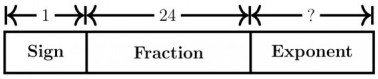
4.27.22 Number Representation: GATE2002-9

https://gateoverflow.in/862

Consider the following $32-bit$ floating-point representation scheme as shown in the format below. A value is specified by 3 fields, a one bit sign field (with 0 for positive and 1 for negative values), a $24bit$ fraction field (with the binary point is at the left end of the fraction bits), and a $7bit$ exponent field (in $excess-64$ signed integer representation, with 16 is the base of exponentiation). The sign bit is the most significant bit.



A. It is required to represent the decimal value -7.5 as a normalized floating point number in the given format. Derive the values of the various fields. Express your final answer in the hexadecimal.
B. What is the largest value that can be represented using this format? Express your answer as the nearest power of 10.

gate2002 digital-logic number-representation normal descriptive

4.27.23 Number Representation: GATE2003-9

https://gateoverflow.in/900

Assuming all numbers are in $2's$ complement representation, which of the following numbers is divisible by 11111011?

A. 11100111 B. 11100100 C. 11010111 D. 11011011

gate2003 digital-logic number-representation normal

4.27.24 Number Representation: GATE2004-19

https://gateoverflow.in/1016

If 73_x (in base-x number system) is equal to 54_y (in base y-number system), the possible values of x and y are

A. $8, 16$ B. $10, 12$ C. $9, 13$ D. $8, 11$

gate2004 digital-logic number-representation easy

4.27.25 Number Representation: GATE2004-28

https://gateoverflow.in/1025

What is the result of evaluating the following two expressions using three-digit floating point arithmetic with rounding?

$(113. + -111.) + 7.51$

$113. + (-111. + 7.51)$

A. 9.51 and 10.0 respectively
B. 10.0 and 9.51 respectively
C. 9.51 and 9.51 respectively
D. 10.0 and 10.0 respectively

gate2004 digital-logic number-representation normal

4.27.26 Number Representation: GATE2004-66

https://gateoverflow.in/1060

Let $A = 11111010$ and $B = 00001010$ be two $8-bit\ 2's$ complement numbers. Their product in $2's$ complement is

A. 11000100 B. 10011100 C. 10100101 D. 11010101

gate2004 digital-logic number-representation easy

4.27.27 Number Representation: GATE2004-IT-42

https://gateoverflow.in/3685

Using a $4-bit\ 2's$ complement arithmetic, which of the following additions will result in an overflow?

i. $1100 + 1100$
ii. $0011 + 0111$
iii. $1111 + 0111$

A. i only B. ii only C. iii only D. i and iii only

gate2004-it digital-logic number-representation normal

4.27.28 Number Representation: GATE2004-IT-43

https://gateoverflow.in/3686

The number $(123456)_8$ is equivalent to

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A. $(A72E)_{16}$ and $(22130232)_4$
B. $(A72E)_{16}$ and $(22131122)_4$
C. $(A73E)_{16}$ and $(22130232)_4$
D. $(A62E)_{16}$ and $(22120232)_4$

gate2004-it digital-logic number-representation normal

4.27.29 Number Representation: GATE2005-16, ISRO2009-18, ISRO2015-2

https://gateoverflow.in/1352

The range of integers that can be represented by an n bit $2's$ complement number system is:

A. -2^{n-1} to $(2^{n-1}-1)$
B. $-(2^{n-1}-1)$ to $(2^{n-1}-1)$
C. -2^{n-1} to 2^{n-1}
D. $-(2^{n-1}+1)$ to $(2^{n-1}-1)$

gate2005 digital-logic number-representation easy isro2009 isro2015

4.27.30 Number Representation: GATE2005-17

https://gateoverflow.in/1353

The hexadecimal representation of $(657)_8$ is:

A. 1AF B. D78 C. D71 D. 32F

gate2005 digital-logic number-representation easy

4.27.31 Number Representation: GATE2005-IT-47

https://gateoverflow.in/3808

$(34.4)_8 \times (23.4)_8$ evaluates to

A. $(1053.6)_8$ B. $(1053.2)_8$ C. $(1024.2)_8$ D. None of these

gate2005-it digital-logic number-representation normal

4.27.32 Number Representation: GATE2006-39

https://gateoverflow.in/1815

We consider the addition of two $2's$ complement numbers $b_{n-1}b_{n-2}\dots b_0$ and $a_{n-1}a_{n-2}\dots a_0$. A binary adder for adding unsigned binary numbers is used to add the two numbers. The sum is denoted by $c_{n-1}c_{n-2}\dots c_0$ and the carry-out by c_{out}. Which one of the following options correctly identifies the overflow condition?

A. $c_{out}\left(\overline{a_{n-1}\oplus b_{n-1}}\right)$
B. $a_{n-1}b_{n-1}\overline{c_{n-1}}+\overline{a_{n-1}}\,\overline{b_{n-1}}c_{n-1}$
C. $c_{out}\oplus c_{n-1}$
D. $a_{n-1}\oplus b_{n-1}\oplus c_{n-1}$

gate2006 digital-logic number-representation normal

4.27.33 Number Representation: GATE2006-IT-7, ISRO2009-41

https://gateoverflow.in/3546

The addition of $4-bit$, two's complement, binary numbers 1101 and 0100 results in

A. 0001 and an overflow
B. 1001 and no overflow
C. 0001 and no overflow
D. 1001 and an overflow

gate2006-it digital-logic number-representation normal isro2009

4.27.34 Number Representation: GATE2007-IT-42

https://gateoverflow.in/3477

$(C012.25)_H - (10111001110.101)_B =$

A. $(135103.412)_o$
B. $(564411.412)_o$
C. $(564411.205)_o$
D. $(135103.205)_o$

gate2007-it digital-logic number-representation normal

4.27.35 Number Representation: GATE2008-6

https://gateoverflow.in/404

Let r denote number system radix. The only value(s) of r that satisfy the equation $\sqrt{121_r} = 11_r$, is/are

A. decimal 10 B. decimal 11 C. decimal 10 and 11 D. any value > 2

gate2008 digital-logic number-representation normal

4.27.36 Number Representation: GATE2008-IT-15

https://gateoverflow.in/3275

A processor that has the carry, overflow and sign flag bits as part of its program status word (PSW) performs addition of the following two $2's$ complement numbers 01001101 and 11101001. After the execution of this addition operation, the status of the carry, overflow and sign flags, respectively will be:

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A. $1,1,0$ B. $1,0,0$ C. $0,1,0$ D. $1,0,1$

gate2008-it digital-logic number-representation normal

4.27.37 Number Representation: GATE2009-5, ISRO2017-57

https://gateoverflow.in/1297

$(1217)_8$ is equivalent to

A. $(1217)_{16}$ B. $(028F)_{16}$ C. $(2297)_{10}$ D. $(0B17)_{16}$

gate2009 digital-logic number-representation isro2017

4.27.38 Number Representation: GATE2010-8

https://gateoverflow.in/2179

P is a 16-bit signed integer. The 2's complement representation of P is $(F87B)_{16}$. The 2's complement representation of $8 \times P$ is

A. $(C3D8)_{16}$ B. $(187B)_{16}$ C. $(F878)_{16}$ D. $(987B)_{16}$

gate2010 digital-logic number-representation normal

4.27.39 Number Representation: GATE2013-4

https://gateoverflow.in/1413

The smallest integer that can be represented by an $8-bit$ number in $2's$ complement form is

A. -256 B. -128 C. -127 D. 0

gate2013 digital-logic number-representation easy

4.27.40 Number Representation: GATE2014-1-8

https://gateoverflow.in/1766

The base (or radix) of the number system such that the following equation holds is_____.

$\frac{312}{20} = 13.1$

gate2014-1 digital-logic number-representation numerical-answers normal

4.27.41 Number Representation: GATE2014-2-8

https://gateoverflow.in/1961

Consider the equation $(123)_5 = (x8)_y$ with x and y as unknown. The number of possible solutions is _____ .

gate2014-2 digital-logic number-representation numerical-answers normal

4.27.42 Number Representation: GATE2015-3-35

https://gateoverflow.in/8494

Consider the equation $(43)_x = (y3)_8$ where x and y are unknown. The number of possible solutions is _____

gate2015-3 digital-logic number-representation normal numerical-answers

4.27.43 Number Representation: GATE2016-1-07

https://gateoverflow.in/39649

The $16-bit$ $2's$ complement representation of an integer is $1111 \quad 1111 \quad 1111 \quad 0101$; its decimal representation is _____

gate2016-1 digital-logic number-representation normal numerical-answers

4.27.44 Number Representation: GATE2016-2-09

https://gateoverflow.in/39546

Let X be the number of distinct 16-bit integers in $2's$ complement representation. Let Y be the number of distinct 16-bit integers in sign magnitude representation Then $X-Y$ is_____.

gate2016-2 digital-logic number-representation normal numerical-answers

4.27.45 Number Representation: GATE2017-1-9

https://gateoverflow.in/118289

When two 8-bit numbers $A_7 \ldots A_0$ and $B_7 \ldots B_0$ in 2's complement representation (with A_0 and B_0 as the least significant bits) are added using a **ripple-carry adder,** the sum bits obtained are $S_7 \ldots S_0$ and the carry bits are $C_7 \ldots C_0$. An overflow is said to have occurred if

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A. the carry bit C_7 is 1
B. all the carry bits $(C_7, \ldots, C_0)$ are 1
C. $\left(A_7 . B_7 . \bar{S_7} + \bar{A_7} . \bar{B_7} . S_7\right)$ is 1
D. $\left(A_0 . B_0 . \bar{S_0} + \bar{A_0} . \bar{B_0} . S_0\right)$ is 1

gate2017-1 digital-logic number-representation

4.27.46 Number Representation: GATE2017-2-1 https://gateoverflow.in/118337

The representation of the value of a $16 - bit$ unsigned integer X in hexadecimal number system is $BCA9$. The representation of the value of X in octal number system is

A. 571244 B. 736251 C. 571247 D. 136251

gate2017-2 digital-logic number-representation

4.27.47 Number Representation: GATE2019-22 https://gateoverflow.in/302826

Two numbers are chosen independently and uniformly at random from the set $\{1, 2, \ldots, 13\}$.

The probability (rounded off to 3 decimal places) that their $4 - bit$ (unsigned) binary representations have the same most significant bit is _____.

gate2019 numerical-answers digital-logic number-representation probability

4.27.48 Number Representation: GATE2019-4 https://gateoverflow.in/302844

In 16-bit 2's complement representation, the decimal number -28 is:

A. 1111 1111 0001 1100
B. 0000 0000 1110 0100
C. 1111 1111 1110 0100
D. 1000 0000 1110 0100

gate2019 digital-logic number-representation

4.27.49 Number Representation: GATE2019-8 https://gateoverflow.in/302840

Consider $Z = X - Y$ where X, Y and Z are all in sign-magnitude form. X and Y are each represented in n bits. To avoid overflow, the representation of Z would require a minimum of:

A. n bits B. $n - 1$ bits C. $n + 1$ bits D. $n + 2$ bits

gate2019 digital-logic number-representation

4.27.50 Number Representation: TIFR2011-A-16 https://gateoverflow.in/20253

A variable that takes thirteen possible values can be communicated using?

A. Thirteen bits.
B. Three bits.
C. $\log_2 13$ bits.
D. Four bits.
E. None of the above.

tifr2011 number-representation

4.27.51 Number Representation: TIFR2019-B-1 https://gateoverflow.in/280494

Which of the following decimal numbers can be exactly represented in binary notation with a finite number of bits ?

A. 0.1 B. 0.2 C. 0.4 D. 0.5 E. All the above

tifr2019 digital-logic number-representation

4.28 Pla (1)

4.28.1 Pla: GATE1990-4-i https://gateoverflow.in/85387

State whether the following statements are TRUE or FALSE with reason:

RAM is a combinational circuit and PLA is a sequential circuit.

gate1990 true-false digital-logic ram pla

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4.29 Prime Implicants (2)

4.29.1 Prime Implicants: GATE1997-5.1

https://gateoverflow.in/2252

Let $f(x, y, z) = \bar{x} + \bar{y}x + xz$ be a switching function. Which one of the following is valid?

A. $\bar{y}x$ is a prime implicant of f
B. xz is a minterm of f
C. xz is an implicant of f
D. y is a prime implicant of f

gate1997 digital-logic normal prime-implicants

4.29.2 Prime Implicants: GATE2004-59

https://gateoverflow.in/1054

Which are the essential prime implicants of the following Boolean function?
$f(a, b, c) = a'c + ac' + b'c$

A. $a'c$ and ac' B. $a'c$ and $b'c$ C. $a'c$ only. D. ac' and bc'

gate2004 digital-logic normal prime-implicants

4.30 Rom (4)

4.30.1 Rom: GATE1993-6.6

https://gateoverflow.in/2285

A ROM is used to store the Truth table for binary multiple units that will multiply two $4 - bit$ numbers. The size of the ROM (number of words $\times$ number of bits) that is required to accommodate the Truth table is M words $\times$ N bits. Write the values of M and N.

gate1993 digital-logic normal rom

4.30.2 Rom: GATE1996-1.21

https://gateoverflow.in/2725

A ROM is used to store the table for multiplication of two 8-bit unsigned integers. The size of ROM required is

A. 256×16
B. $64K \times 8$
C. $4K \times 16$
D. $64K \times 16$

gate1996 digital-logic normal rom

4.30.3 Rom: GATE2004-IT-10

https://gateoverflow.in/3651

What is the minimum size of ROM required to store the complete truth table of an $8 - bit \times 8 - bit$ multiplier?

A. $32K \times 16$ bits
B. $64K \times 16$ bits
C. $16K \times 32$ bits
D. $64K \times 32$ bits

gate2004-it digital-logic normal rom

4.30.4 Rom: GATE2012-19

https://gateoverflow.in/51

The amount of ROM needed to implement a $4 - bit$ multiplier is

A. 64 bits B. 128 bits C. 1 Kbits D. 2 Kbits

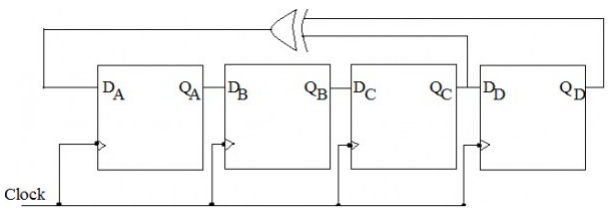
gate2012 digital-logic normal rom

4.31 Shift Registers (1)

4.31.1 Shift Registers: GATE1987-13-a

https://gateoverflow.in/82607

The below figure shows four D-type flip-flops connected as a shift register using a XOR gate. The initial state and three subsequent states for three clock pulses are also given.



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State	Q_A	Q_B	Q_C	Q_D
Initial	1	1	1	1
After the first clock	0	1	1	1
After the second clock	0	0	1	1
After the third clock	0	0	0	1

The state $Q_AQ_BQ_CQ_D$ after the fourth clock pulse is

A. 0000 B. 1111 C. 1001 D. 1000

gate1987 digital-logic circuit-output shift-registers

4.32 Static Hazard (1)

4.32.1 Static Hazard: GATE2006-38

https://gateoverflow.in/1814

Consider a Boolean function $f(w,x,y,z)$. Suppose that exactly one of its inputs is allowed to change at a time. If the function happens to be true for two input vectors $i_1 = \langle w_1, x_1, y_1, z_1 \rangle$ and $i_2 = \langle w_2, x_2, y_2, z_2 \rangle$, we would like the function to remain true as the input changes from i_1 to i_2 (i_1 and i_2 differ in exactly one bit position) without becoming false momentarily. Let $f(w,x,y,z) = \sum(5,7,11,12,13,15)$. Which of the following cube covers of f will ensure that the required property is satisfied?

A. $\overline{w}xz, wx\overline{y}, x\overline{y}z, xyz, wyz$
B. $wxy, \overline{w}xz, wyz$
C. $wx\overline{y}\overline{z}, xz, w\overline{x}yz$
D. $wx\overline{y}, wyz, wxz, \overline{w}xz, x\overline{y}z, xyz$

gate2006 digital-logic min-sum-of-products-form normal static-hazard

4.33 Synchronous Asynchronous Circuits (4)

4.33.1 Synchronous Asynchronous Circuits: GATE1991-03-ii

https://gateoverflow.in/516

Choose the correct alternatives (more than one may be correct) and write the corresponding letters only:

Advantage of synchronous sequential circuits over asynchronous ones is:

A. faster operation
B. ease of avoiding problems due to hazards
C. lower hardware requirement
D. better noise immunity
E. none of the above

gate1991 digital-logic normal synchronous-asynchronous-circuits

4.33.2 Synchronous Asynchronous Circuits: GATE1998-16

https://gateoverflow.in/1730

Design a synchronous counter to go through the following states:

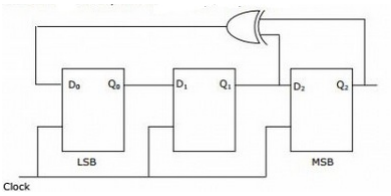
$$1, 4, 2, 3, 1, 4, 2, 3, 1, 4 \ldots$$

gate1998 digital-logic normal descriptive synchronous-asynchronous-circuits

4.33.3 Synchronous Asynchronous Circuits: GATE2001-2.12

https://gateoverflow.in/730

Consider the circuit given below with initial state $Q_0 = 1, Q_1 = Q_2 = 0$. The state of the circuit is given by the value $4Q_2 + 2Q_1 + Q_0$



Which one of the following is correct state sequence of the circuit?

A. $1, 3, 4, 6, 7, 5, 2$
B. $1, 2, 5, 3, 7, 6, 4$
C. $1, 2, 7, 3, 5, 6, 4$
D. $1, 6, 5, 7, 2, 3, 4$

gate2001 digital-logic normal synchronous-asynchronous-circuits

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4.33.4 Synchronous Asynchronous Circuits: GATE2003-44

https://gateoverflow.in/935

A 1-input, 2-output synchronous sequential circuit behaves as follows:

Let z_k, n_k denote the number of $0'$s and $1's$ respectively in initial k bits of the input $(z_k + n_k = k)$. The circuit outputs 00 until one of the following conditions holds.

- $z_k - n_k = 2$. In this case, the output at the k-th and all subsequent clock ticks is 10.
- $n_k - z_k = 2$. In this case, the output at the k-th and all subsequent clock ticks is 01.

What is the minimum number of states required in the state transition graph of the above circuit?

A. 5 B. 6 C. 7 D. 8

gate2003 digital-logic synchronous-asynchronous-circuits normal

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